JVC

SERVICE MANUAL

MICRO COMPONENT MD SYSTEM

UX-A10DVD
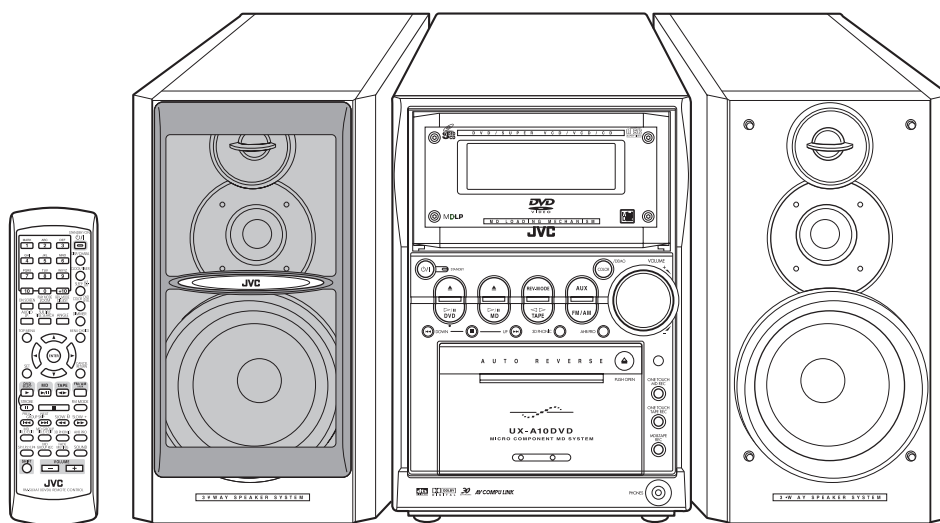
Area suffix

UB ----------- Hong Kong

Contents

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.

2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.

3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.

4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.

5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.

   ● Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).

   ● Alternate check method
   Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500 Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
   Measure the AC voltage across the resistor with the AC voltmeter.
   Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. Voltage measured any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).

AC VOLTMETER
(Having 1000 ohms/volts, or more sensitivity)

0.15μF AC TYPE

Place this probe on each exposed metal part.

1500 Ω 10W

Good earth ground
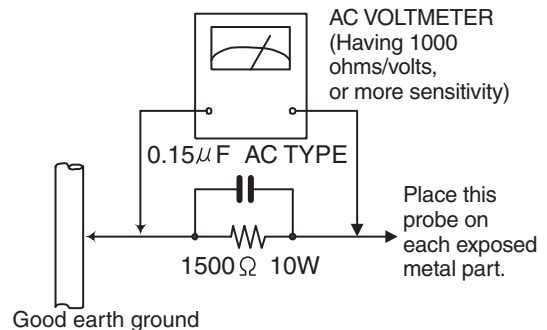
Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ CAUTION

Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▬) and ICP (●) or identified by the "⚠" mark nearby are critical for safety.

(This regulation does not correspond to J and C version.)

Preventing static electricity

1.Grounding to prevent damage by static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

## 2.About the earth processing for the destruction prevention by static electricity

Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as CD players. Be careful to use proper grounding in the area where repairs are being performed.

2-1 Ground the workbench

Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

2-2 Ground yourself

Use an anti-static wrist strap to release any static electricity built up in your body.

(caption)
Anti-static wrist strap

1MΩ
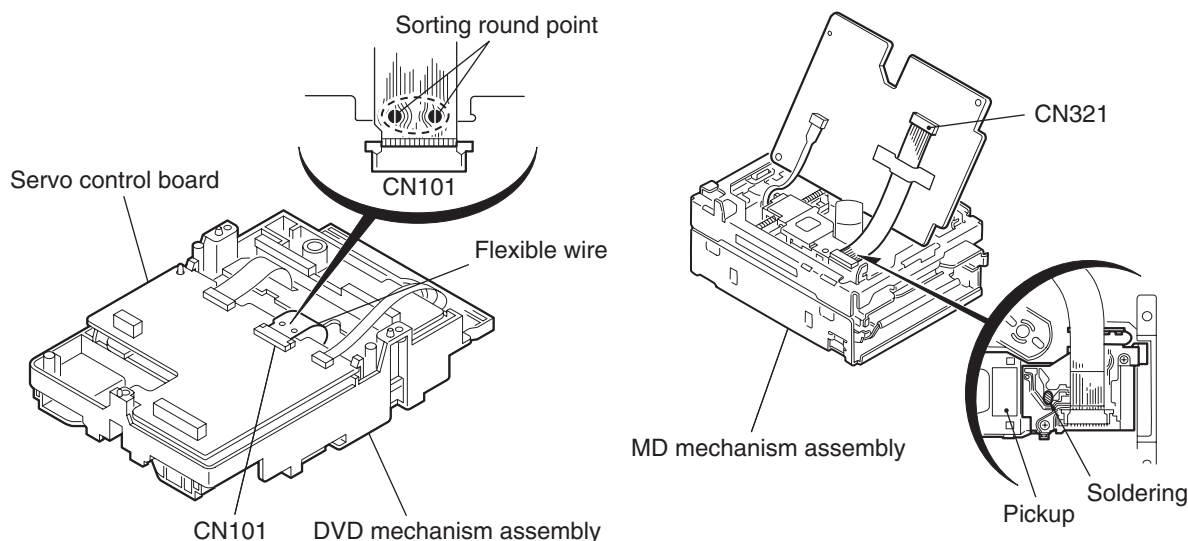
Conductive material
(conductive sheet) or iron plate
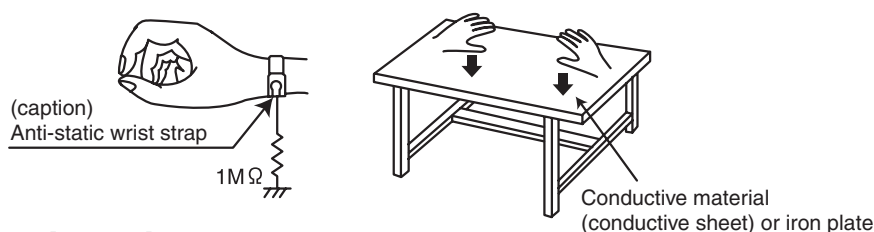
3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

Attention when traverse unit is decomposed

*Please refer to "Disassembly method" in the text for pick-up and how to detach the substrate.

1.Solder is put up before the card wire is removed from connector on the CD substrate as shown in Figure. (When the wire is removed without putting up solder, the pick-up assembly might destroy.)
2.Please remove solder after connecting the card wire with when you install picking up in the substrate.

Sorting round point

CN101

Servo control board

Flexible wire

CN321

CN101   DVD mechanism assembly

MD mechanism assembly

Soldering

Pickup

Disassembly method

<Main body>

■ Removing the metal cover (See Fig.1~3)

1. Remove the six screws **A** on the back of the body.

2. Remove the screw **B** on each side of the body.

3. Detach the rear side of the metal cover upward while pulling the lower sides outward.
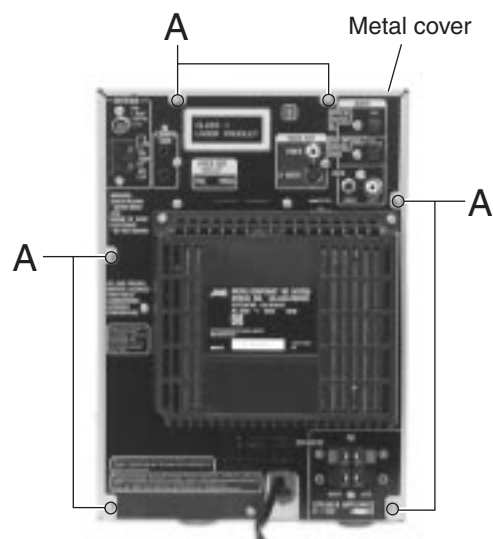
Fig.1
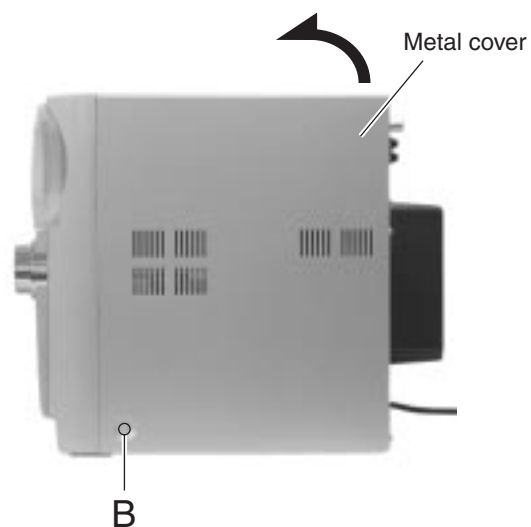
Fig.2
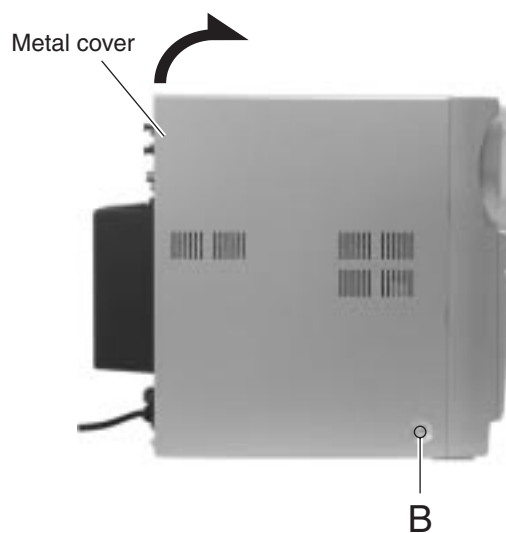
Fig.3

■ Removing the DVD mechanism assembly (See Fig.4~6)

- ・ Prior to performing the following procedure, remove the metal cover.

1. Remove the three screws **C** attaching the DVD mechanism assembly on top of the body.

2. Disconnect connector CN502 and CN503 on the DVD servo board upward at the bottom of the DVD mechanism assembly.
   Bring up the DVD mechanism assembly and remove backward.

DVD mechanism assembly

Fig.4

C   C

DVD mechanism assembly

CN502

CN503

C

Fig.5

DVD mechanism assembly
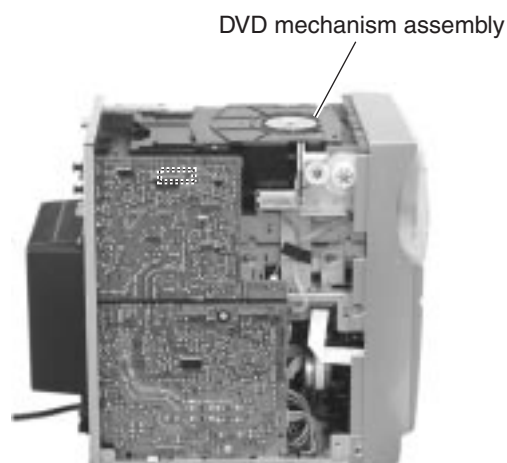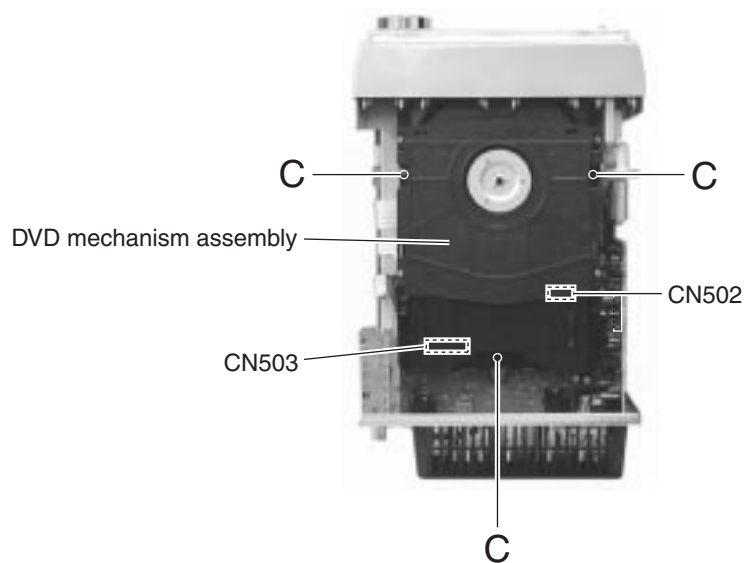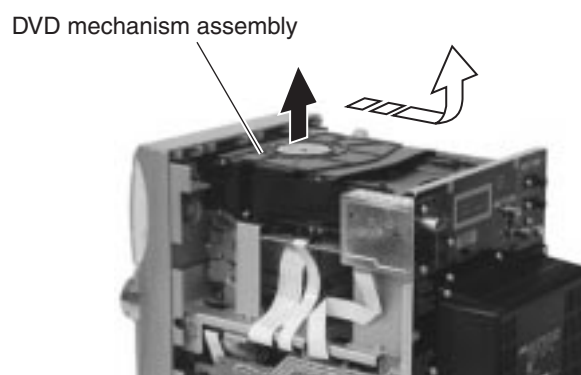
Fig.6

■Removing the front panel assembly
(See Fig.7~10)

・ Prior to performing the following procedure, remove the metal cover and the DVD mechanism assembly.

1. Disconnect the card wire from connector CN705 on the microcomputer board in the center of the right side of the body.

2. Disconnect the card wire from connector CN301 on the main board in the center of the left side of the body.

3. Disconnect the card wire from connector CN704, and the wires from CN703 and CN710 on the microcomputer board.

> ATTENTION: When disconnecting the wires from CN703 and CN710, remove the spacer attaching the wires.

4. Disconnect the card wire from connector CN442 on the FL connection board on top of the body.

5. Remove the screw **D** on each side of the body.

6. Remove the two screws **E** on the bottom of the body.

7. Release the joint **a** on the bottom and the two joints **b** on the right and left sides of the body using a screwdriver. Remove the front panel assembly toward the front.

Front panel assembly

D

b

Microcomputer board
CN705

Fig.7

CN710   Front panel assembly

Spacer

D

CN703   b   Microcomputer board
CN704

Main board
CN301

Fig.8

FL connection board
CN442   Front panel assembly

Spacer

CN710   CN703   Microcomputer board
CN704

Fig.9

E   E   Front panel assembly

a
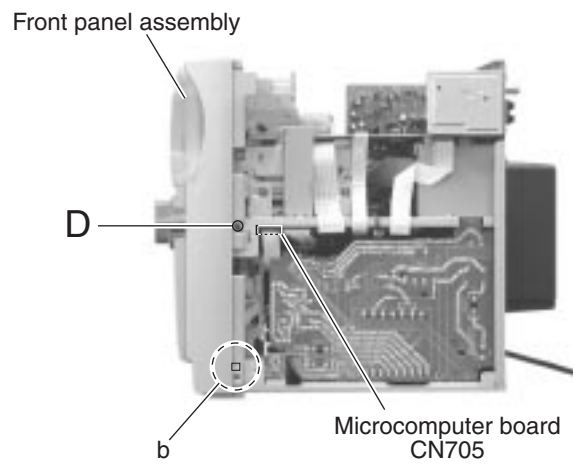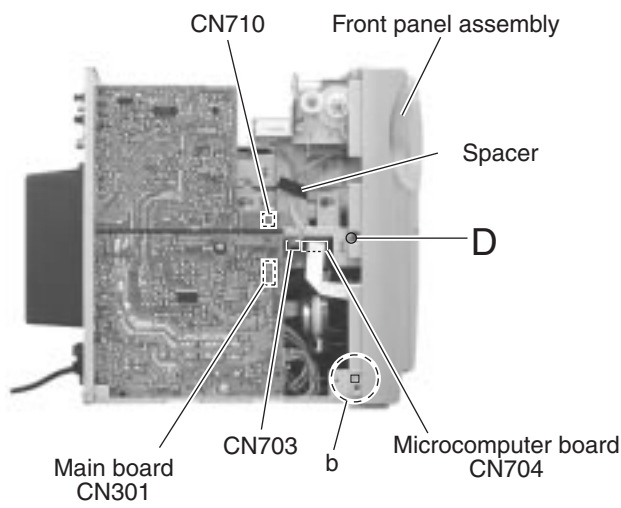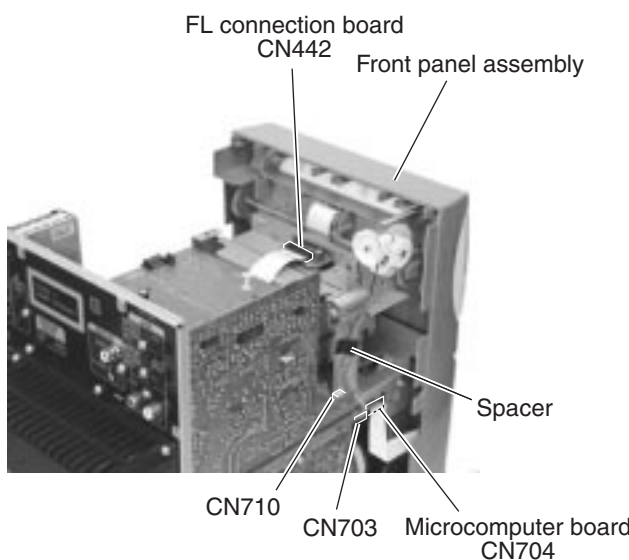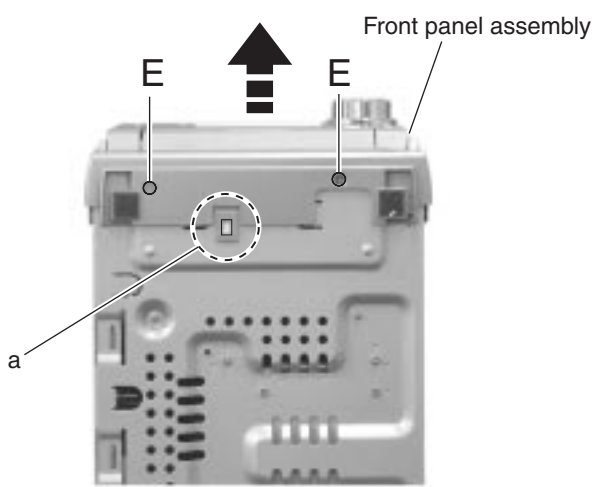
Fig.10

■ Removing the rear cover/ rear panel
(See Fig.11~15)

・ Prior to performing the following procedure, remove the metal cover and the DVD mechanism assembly.

1. Remove the two screws **F** on the back of the body.

2. Disconnect the wire from connector CN1 on the tuner pack on the right side of the body.

3. Remove the thirteen screws **G** on the back of the body.

4. Release the two joints **c** on the lower right and left sides of the rear panel.

> REFERENCE:The rear panel with the tuner pack comes off.

Rear panel

F   F

Rear cover

Fig.11

Rear panel

Tuner pack
CN1

Fig.12

G

G   G

G

G

Rear panel

G

FIg.13

Rear panel

c

Fig.14

Rear panel   c
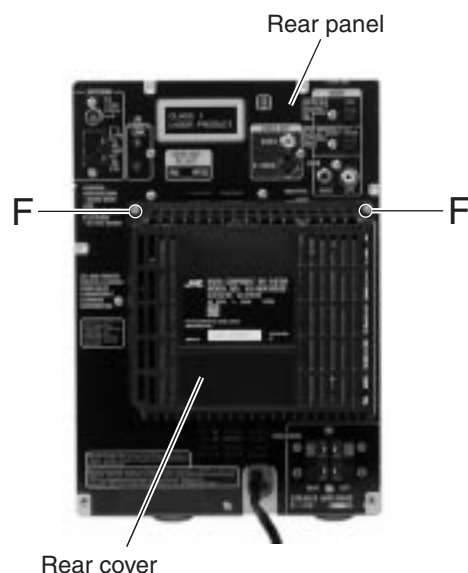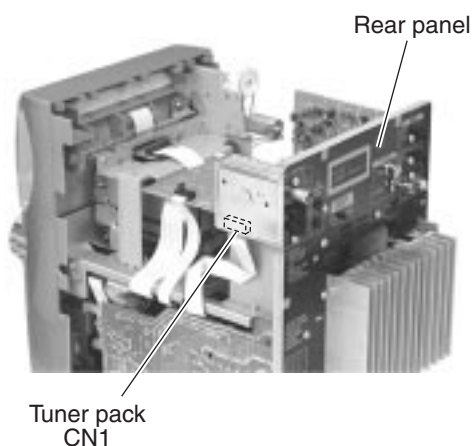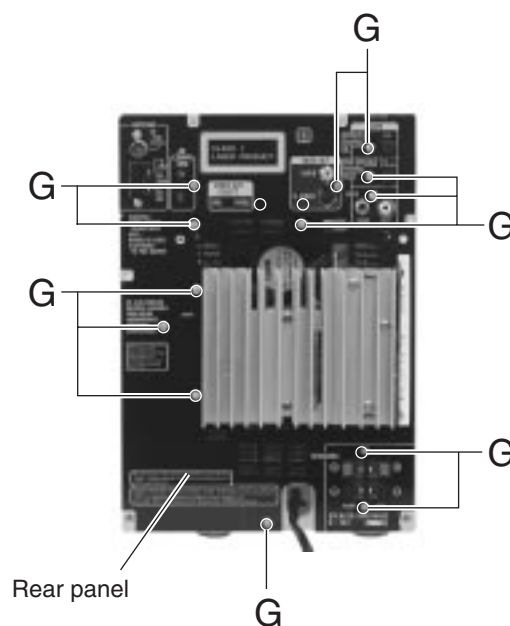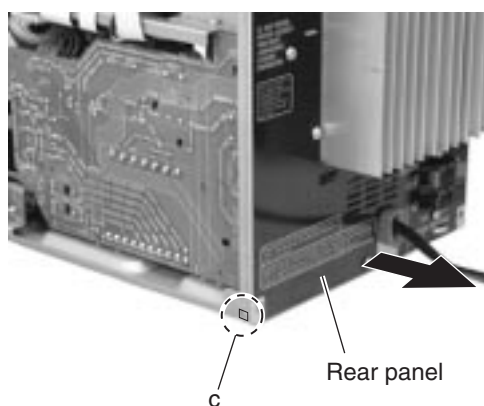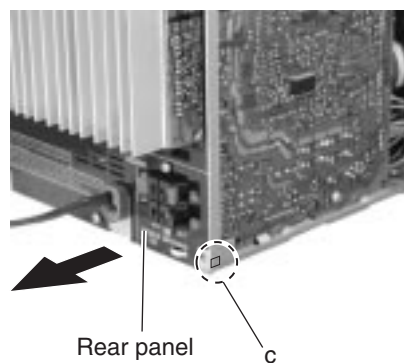
Fig.15

■Removing the tuner pack   (See Fig.16)

・ Prior to performing the following procedure, remove the metal cover.

1. Disconnect the card wire from connector CN1 on the tuner pack on the right side of the body.

2. Remove the two screws **H** on the back of the body.

Tuner pack

H

CN1

Fig.16

■Removing the fan   (See Fig.17,18)

・ Prior to performing the following procedure, remove the metal cover, the DVD mechanism assembly, the rear cover/rear panel and the DVD relay board.

1. Disconnect the wire from connector CN711 on the microcomputer board on the right side of the body.

2. Remove the three screws **I** attaching the fan bracket on top of the body and release the joint **d**.

3. Remove the two screws **J** attaching the fan.

CN711

I

d

I

Fan bracket

Fig.17

Fan bracket

J

Fig.18   Fan
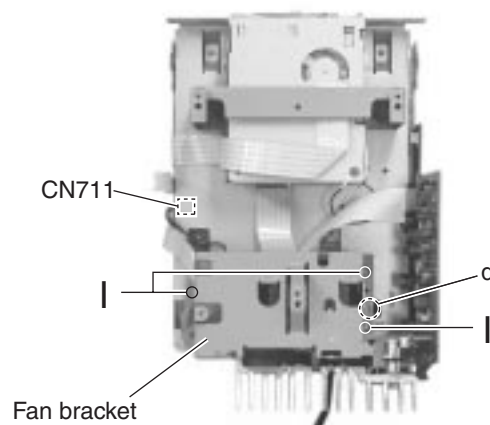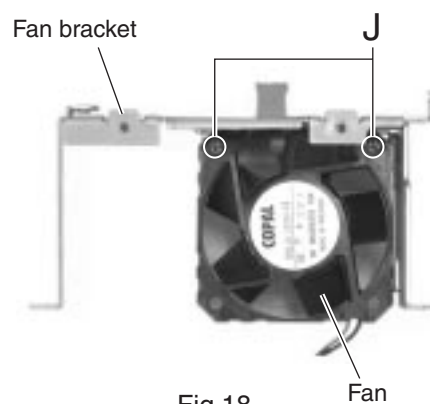
■ Removing the MD mechanism assembly
(See Fig.19~21)

・ Prior to performing the following procedure, remove the metal cover, the DVD mechanism assembly and the front panel assembly.

1. Remove the two screws **K** attaching the DVD mechanism attaching bracket.

2. Remove the two screws **L** on each side of the MD mechanism assembly and remove the MD mechanism assembly toward the front.

3. Disconnect the card wire from connector CN521 on the MD mechanism assembly board.
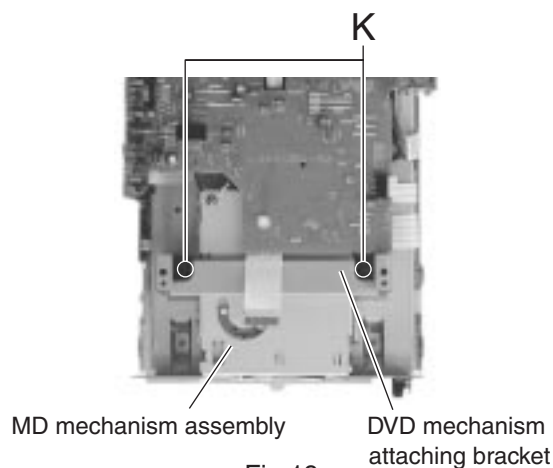
■ Removing the headphone board
(See Fig.22,23)

・ Prior to performing the following procedure, remove the metal cover, the DVD mechanism assembly and the front panel assembly.

1. Disconnect the wire from connector CN310 on the main board on the left side of the body.

2. Release the wires from the two clamps on the bottom chassis.

3. Remove the screw **M** attaching the headphone board on the right side of the body.

K

MD mechanism assembly   DVD mechanism attaching bracket

Fig.19

DVD mechanism attaching bracket
MD mechanism assembly
L
L

Fig.20

MD mechanism assembly
CN521

Fig.21

Headphone board
Main board CN310
Clamp

Fig.22

Headphone board   M

Fig.23

1-9
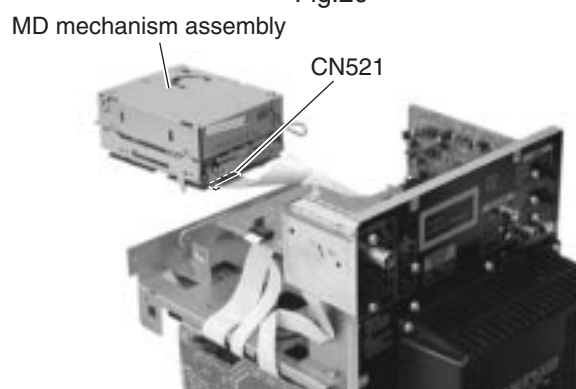
■Removing the main board
(See Fig.24,25)

• Prior to performing the following procedure, remove the metal cover, the DVD mechanism assembly, the front panel assembly and the rear cover/ rear panel.

1. Remove the two screws **N** and the three screws **O**. Remove the heat sink.

2. Disconnect the wires from connector CN307 and CN310, the card wire from CN312 on the main board on the left side of the body.

3. Remove the screw **P** and **Q** attaching the main board.

4. Disconnect connector CN303, CN304, CN305 and CN306 on the main board. Release the two joints **e** at the bottom.

5. Draw out the main board and disconnect the card wire and the wire from connector CN302 and CN311.
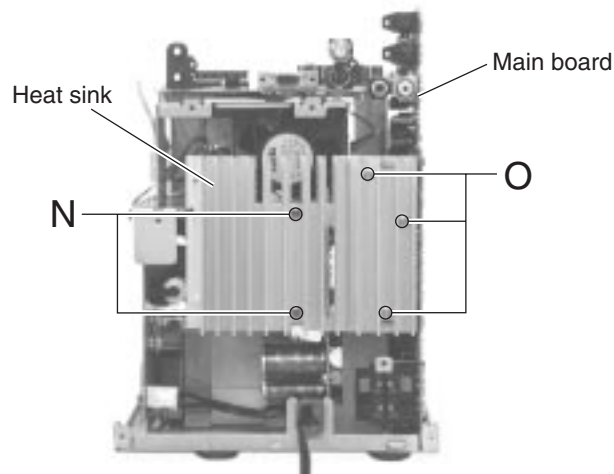
Fig.24
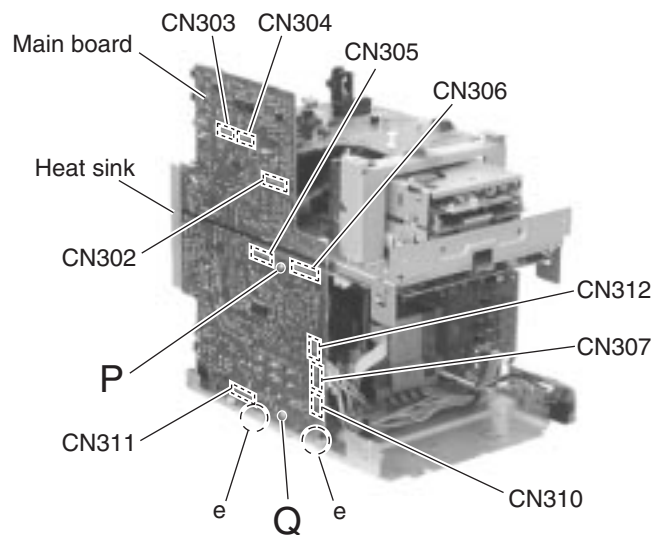
Fig.25

■Removing the DVD relay board
(See Fig.26)

• Prior to performing the following procedure, remove the metal cover, the DVD mechanism assembly and the rear panel/ rear cover.

1. Disconnect the card wire from connector CN515 on the DVD relay board.

2. Remove the screw **R** attaching the DVD relay board on top of the body.

3. Disconnect connector CN511 and CN512 on the DVD relay board.
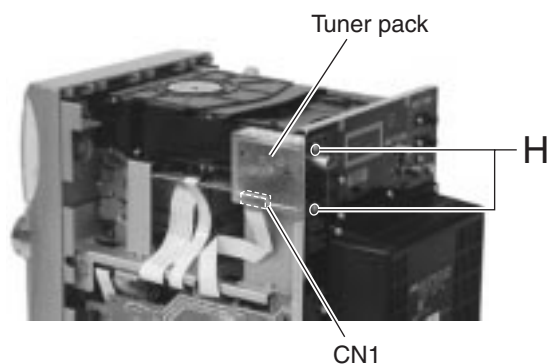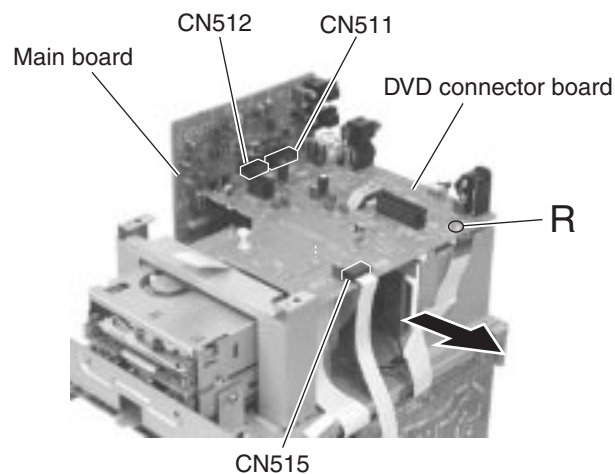

Fig.26

■Removing the MD base chassis/ microcomputer board   (See Fig.27~29)

· Prior to performing the following procedure, remove the metal cover, the DVD mechanism assembly, the front panel assembly, the rear cover/ rear panel, the main board and the DVD relay board.

REFERENCE: It is not necessary to remove the DVD mechanism assembly.

1. Disconnect the wire from connector CN701 on the microcomputer board in the center of the right side of the body.

2. Remove the two screws **S** attaching the MD base chassis on top of the body.

3. Disconnect connector CN706 and CN707 on the microcomputer board from the main board.

REFERENCE: The MD base chassis with the MD mechanism assembly comes off.

4. Remove the two screws **T** attaching the microcomputer board and release the two joints **f**.

MD mechanism assembly   MD base chassis

Microcomputer board
CN701

Fig.27

MD mechanism assembly   MD base chassis

CN706

CN707

S

Fan bracket   Main board

Fig.28

T

Microcomputer board

CN706

CN707

f
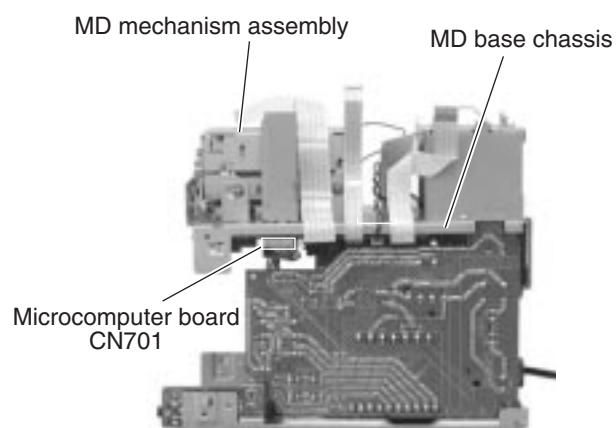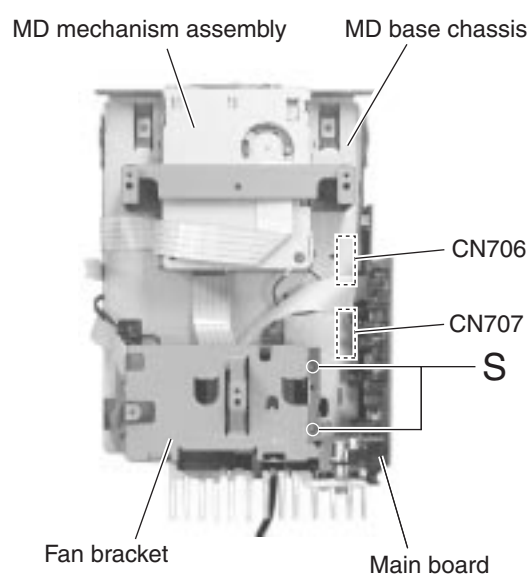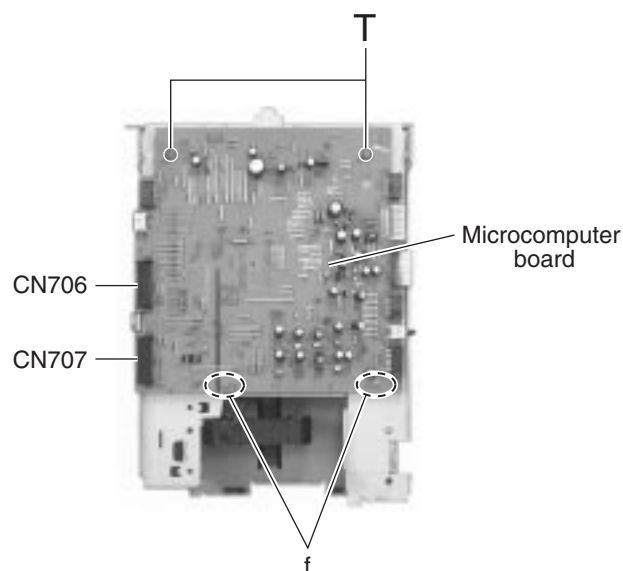
Fig.29

■**Removing the power transformer assembly (See Fig.30,31)**

· Prior to performing the following procedure, remove the metal cover, the DVD mechanism assembly, the front panel assembly, the rear cover/ rear panel, the main board and the MD base chassis.

1. Move the power cord stopper upward on the back of the body and remove. Disconnect the power cord from connector CN901 on the power transformer board.

> REFERENCE: The power cord can be removed alone.

2. Remove the four screws **U** on top of the body and release the wires from the two clamps on the bottom chassis.
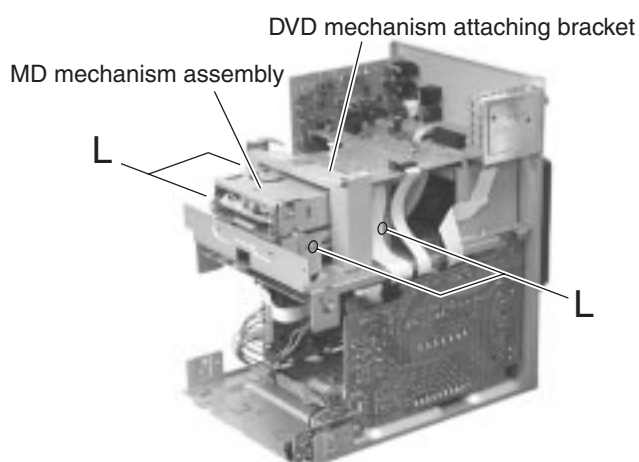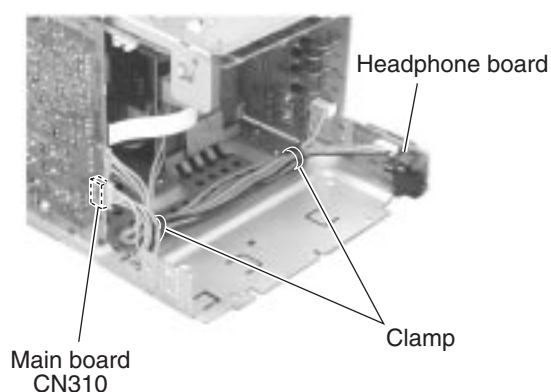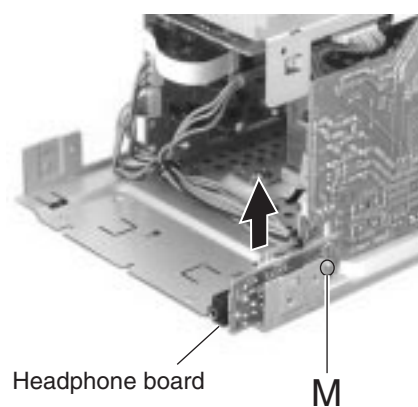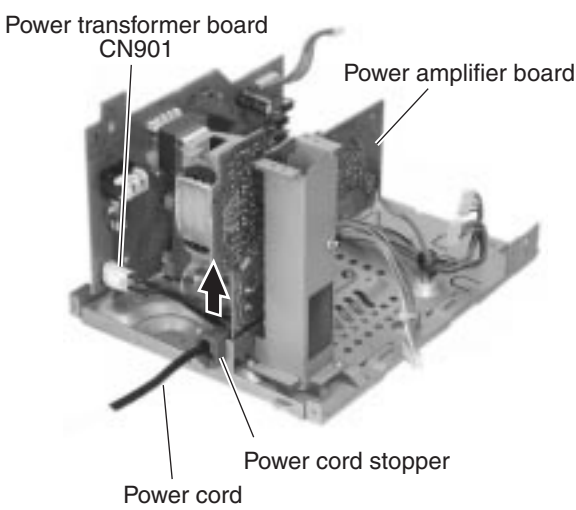
■**Removing the power amplifier board (See Fig.32,33)**

· Prior to performing the following procedure, remove the metal cover, the DVD mechanism assembly, the front panel assembly, the rear cover/ rear panel, the main board and the MD base chassis.

1. Disconnect the wire from connector CN111 on the power amplifier board.

2. Remove the band attaching the wire to the power amplifier board.

3. Release the wires from the clamp.

4. Move the power amplifier board upward to release the two joints **g** and remove to the right.

Power transformer board CN901
Power amplifier board
Power cord stopper
Power cord

Fig.30

Clamp   Bottom chassis
U   U
Power transformer assembly
U

Fig.31

Band   Power amplifier board CN111

Fig.32

Power amplifier board
g
Band
Clamp
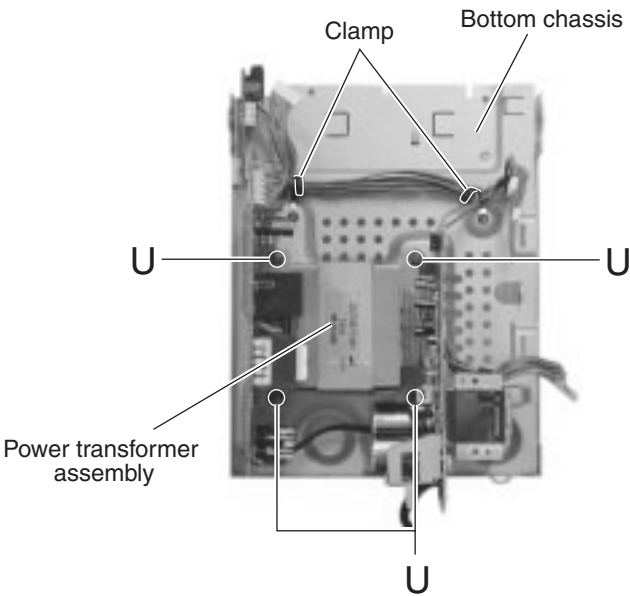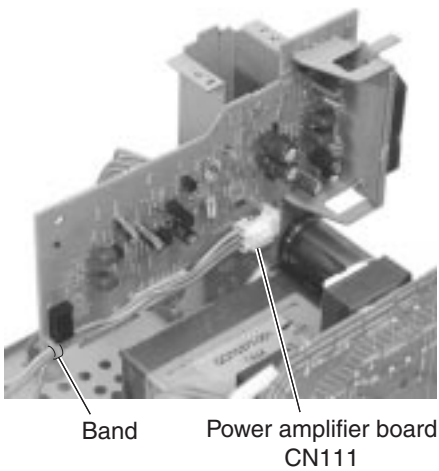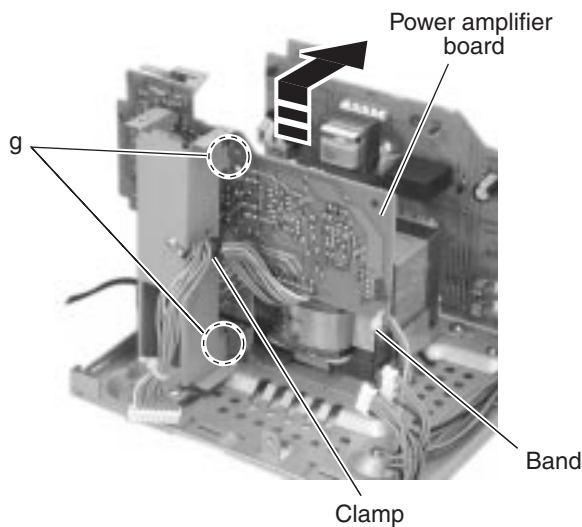
Fig.33

<Front panel assembly>

・ Prior to performing the following procedure, remove the metal cover, the DVD mechanism assembly and the front panel assembly.

■ Removing the cassette mechanism assembly (See Fig.34,35)

1. Remove the spring attached to the cassette door on the back of the front panel.

2. Remove the four screws **V** attaching the cassette mechanism assembly.

Cassette door

Spring
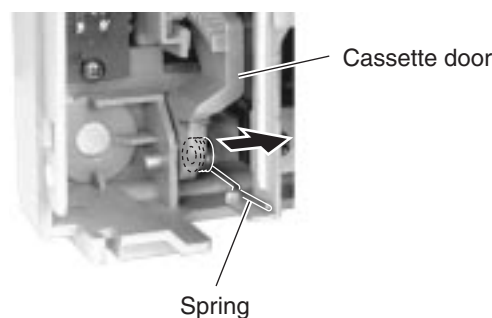
Fig.35

■ Removing the key board (See Fig.36~38)

・ Prior to performing the following procedure, remove the cassette mechanism assembly.

1. Pull out the volume knob on the front side of the front panel.

2. Remove the five screws **W** attaching the bracket (1) on the back of the front panel.

3. Remove the ten screws **X** attaching the key board.

V   Cassette mechanism assembly

V

Spring

V

Fig.34

Front panel assembly

Volume knob

Fig.36

Bracket(1)

W

W

W

Front panel

Fig.37

X   Key board

X

X

X
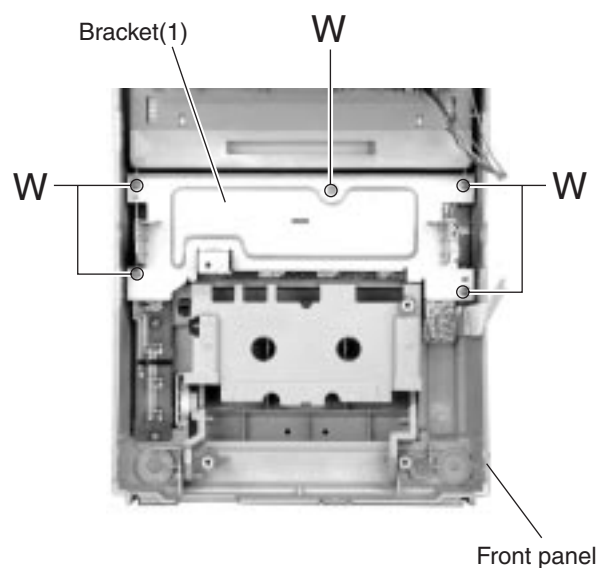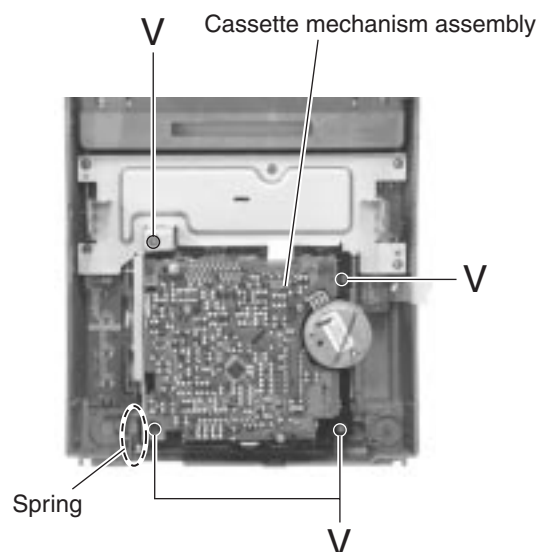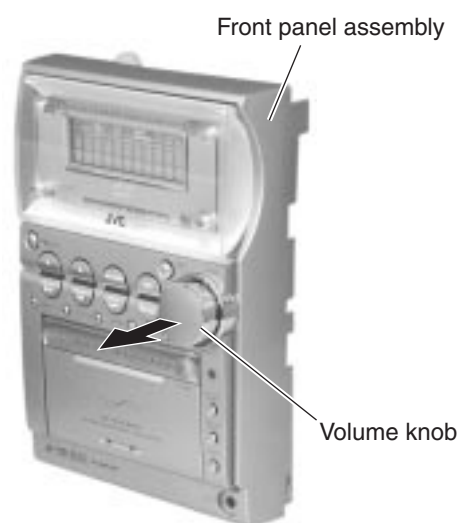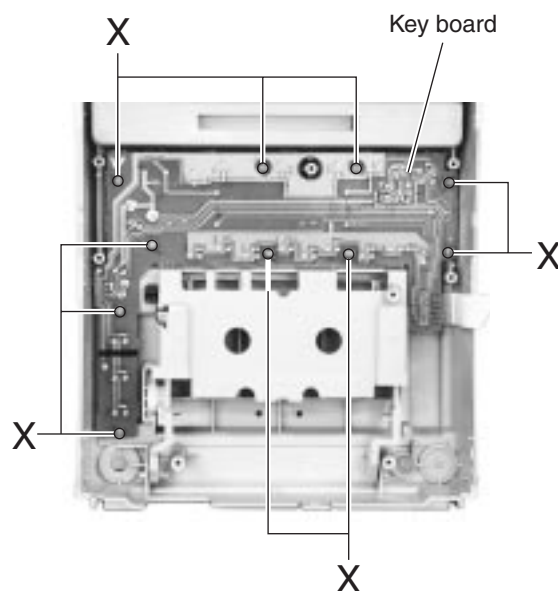
Fig.38

■Removing the FL connection board
(See Fig.39~41)

1. Remove the two screws **Y** and the screw **Z** attaching the bracket (2) on the back of the front panel.

2. Disconnect the card wire from connector CN441 on the FL connection board.

3. Push the two joint tabs **h** downward to release and pull out the FL connection board.

FL connection board
CN441   Y   Front panel

Y
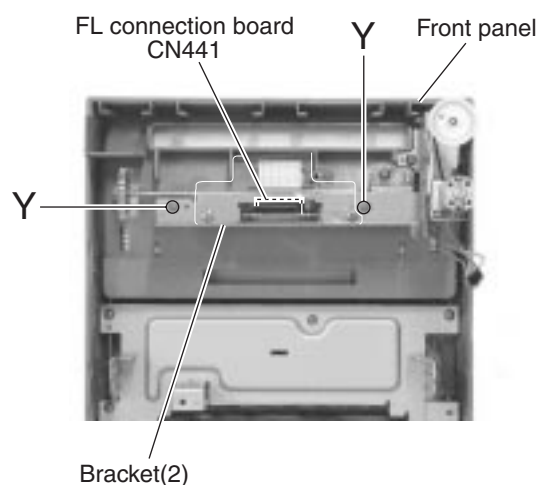
Bracket(2)

Fig.39

■Removing the Drive motor assembly
(See Fig.39, 40,42)

1. Remove the two screws **Y** and the screw **Z** attaching the bracket (2) on the back of the front panel.

2. Remove the screw **A'** attaching the drive motor assembly. Release the joint tab **i** and pull out the drive motor assembly.

Bracket(2)   Front panel

Drive motor   Z

Fig.40

CN441   h

h

FL connection board

Fig.41

A'

Drive motor

i
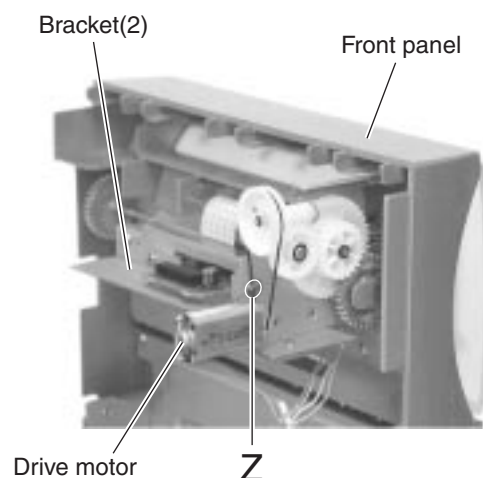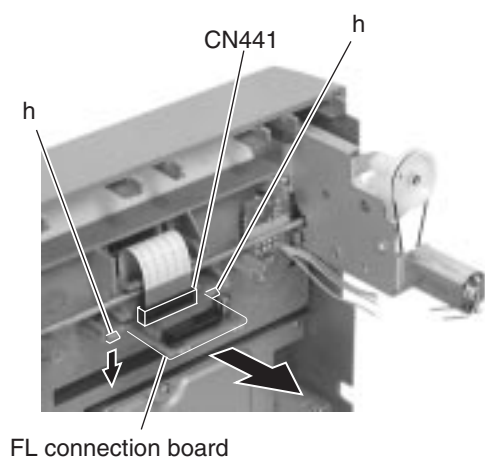
Fig.42

■Removing the belt/ drive motor
(See Fig.43)

・ Prior to performing the following procedure, remove the drive motor assembly.

1. Remove the belt from the pulley

2. Remove the two screws **B'** attaching the drive motor.

Belt

Drive motor

B'

Fig.43

■Removing the switch board
(See Fig.44,45)

・ Prior to performing the following procedure, remove the bracket (2) / drive motor assembly.

1. Disconnect the card wire from connector CN441 on the FL connection board(Do not fold down the card wire).

2. Release the joint **j** and **k** in order on the right and left sides of the shaft gear.

   Remove the screw **C'** attaching the switch board and release the joint tab **l**.

k

FL connection board
CN441

Switch board

Shaft gear

j

Fig.44

C'

Switch board

l
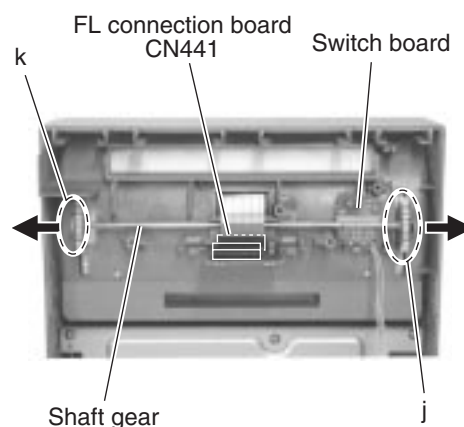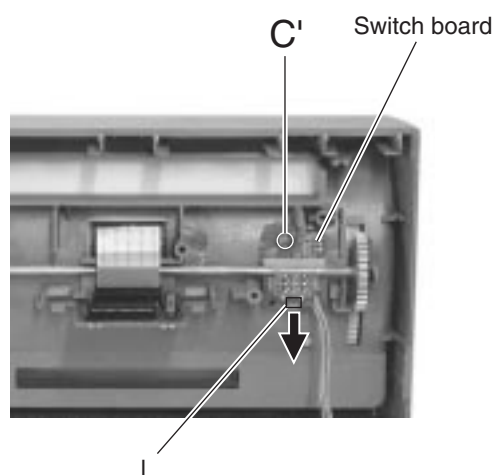
Fig.45

■Removing the FL display section
(See Fig.46~51)

1. Remove the four screws **D'** attaching the case cover on the front panel.

2. Pull out the FL panel from the four joint bosses **m** on the FL display cover.

3. Remove the four screws **E'** attaching the FL display cover. Disconnect the card wire from connector CN451 on the FL relay board and from CN452 on the LED board.

D'
Case cover
D'

Fig.46

m
FL panel
m

Fig.47

FL display cover

E'
E'

Fig.48

FL connection board
CN451
LED board
CN452
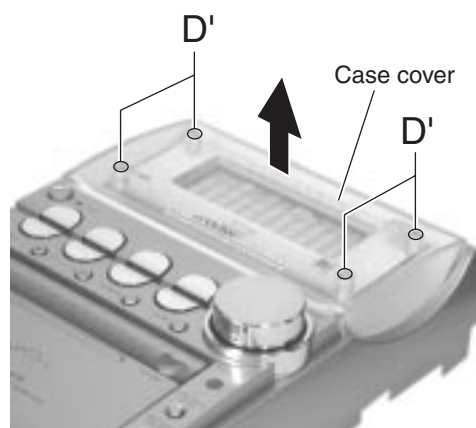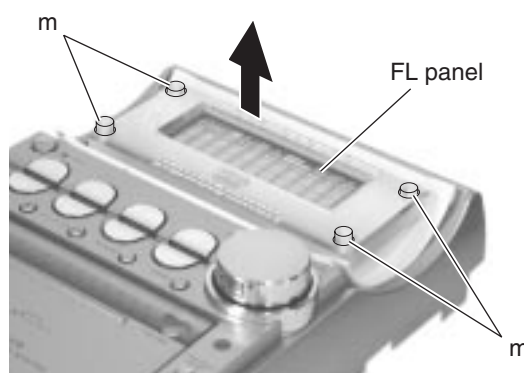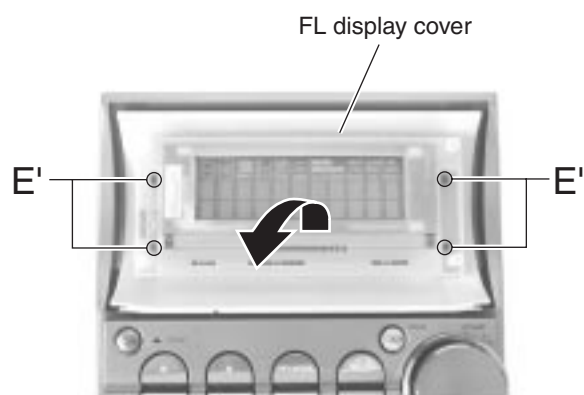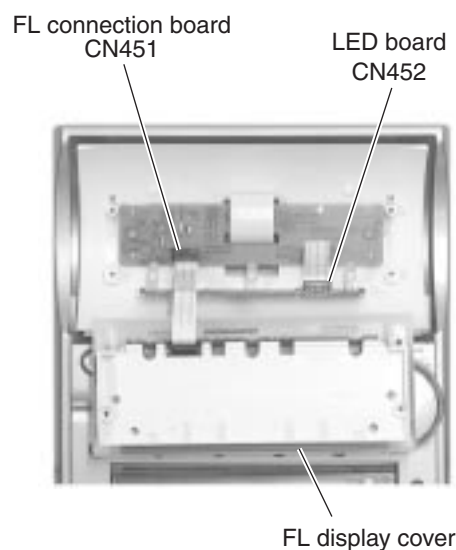
FL display cover

Fig.49

4. Remove the two screws **F'** attaching the FL display on the FL display cover.

5. The FL board and the lens come off from the FL display section.

FL display section FL display cover

F'   F'

Fig.50

FL display section

LED board

FL board   Lens
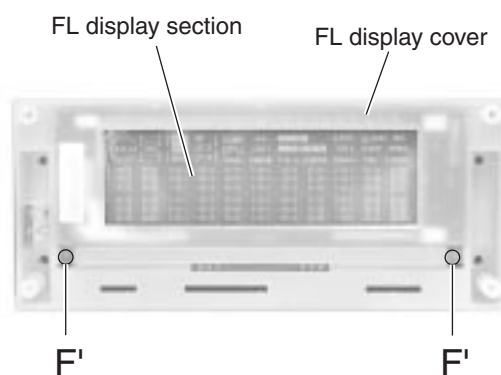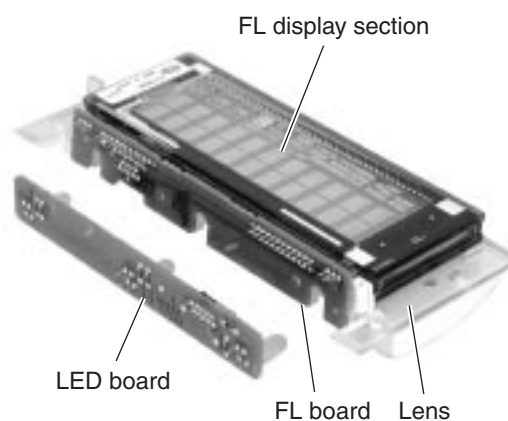
Fig.51

■ Removing the FL relay board(See Fig.52)

・ Prior to performing the following procedure, remove the FL display cover.

1. Disconnect the card wire from connector CN453 on the FL relay board.

2. Remove the two screws **G'** attaching the FL relay board.

CN453   FL connection board

G'   G'
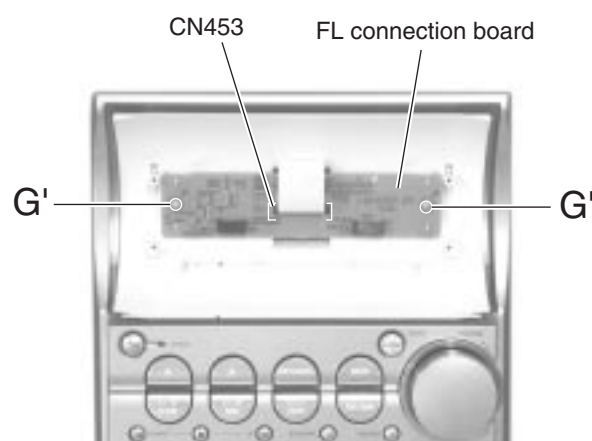
Fig.52

<DVD loading mechanism section>

■Removing the clamper assembly
(See Fig.1)

1. Remove the four screws **A** attaching the clamper assembly.

2. Move the clamper assembly in the direction of the arrow to release the joint **a** on each side, and remove.

> ATTENTION: When reassembling, reattach the clamper assembly at the two joints **a**.
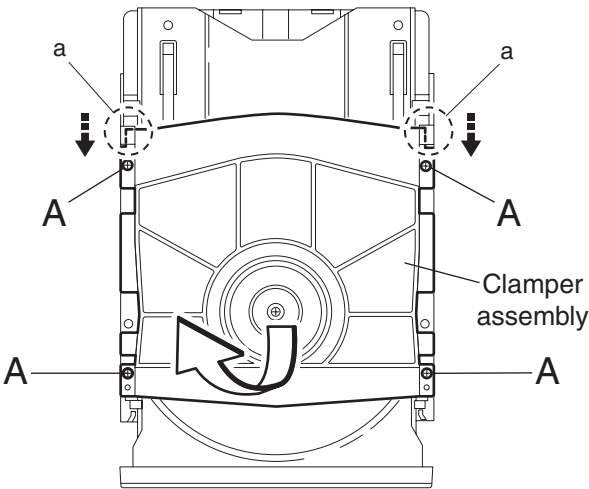
■Removing the tray　　　　(See Fig.2,3)

・ Prior to performing the following procedure, remove the clamper assembly.

1. Push the part b of the slide cam through the slot on the left side of the loading base.

2. Draw out the tray toward the front.

> ATTENTION: When reattaching the tray, move the part c of the slide cam to the right(See Fig.3).
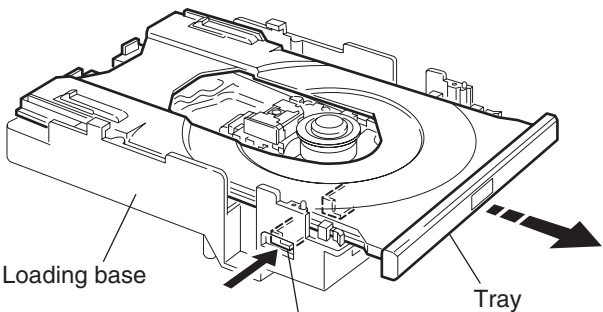
■Removing the servo control board
(See Fig.4)

> CAUTION: Solder the sorting round point before disconnecting the flexible wire extending from the pickup. If you do not follow this instruction, the pickup may be damaged.

1. Solder the sorting round point on the flexible wire connected to connector CN101 on the servo control board.

2. Disconnect the flexible wire from connector CN101 on the servo control board.

3. Disconnect the card wires from connector CN201 and CN202 on the servo control board.

4. Release the two joints d.

5. Move the servo control board in the direction of the arrow to release the joint e, and remove upward.

> CAUTION: Unsolder the sorting round point after reassembling.

Fig.1

Fig.2
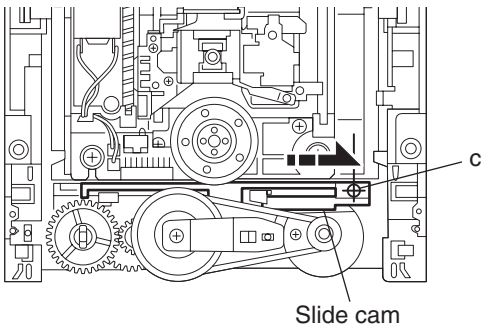
Fig.3
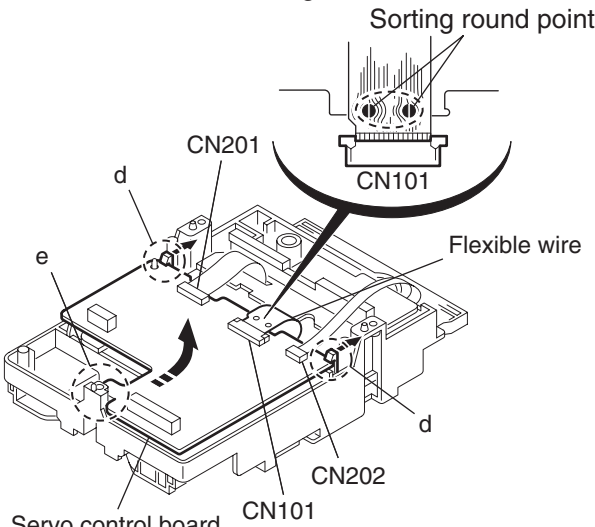
Fig.4

■ Removing the traverse mechanism assembly (See Fig.5,6)

・ Prior to performing the following procedure, remove the clamper assembly, the tray and the servo control board.

1. Remove the four screws **B** attaching the traverse mechanism assembly.

CAUTION: When reassembling, get the flexible wire extending from the spindle motor board through the slot f of the elevator.
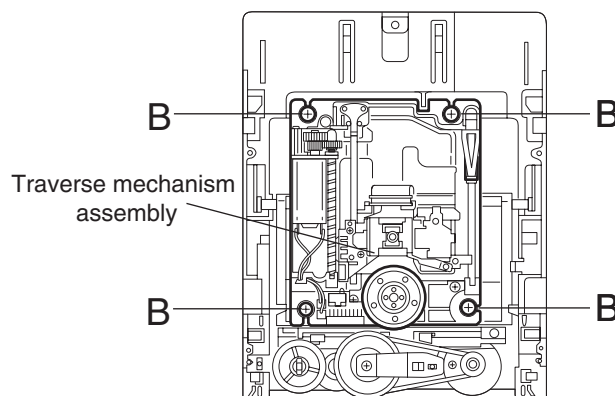
Fig.5

■ Removing the elevator (See Fig.7 and 8)

・ Prior to performing the following procedure, remove the clamper assembly, the tray, the servo control board and the traverse mechanism assembly.

1. Pull the two tabs **g** outward and release the two shafts of the elevator.

ATTENTION: When reassembling, fit the two shafts on the front side of the elevator into the grooves h of the slide cam.
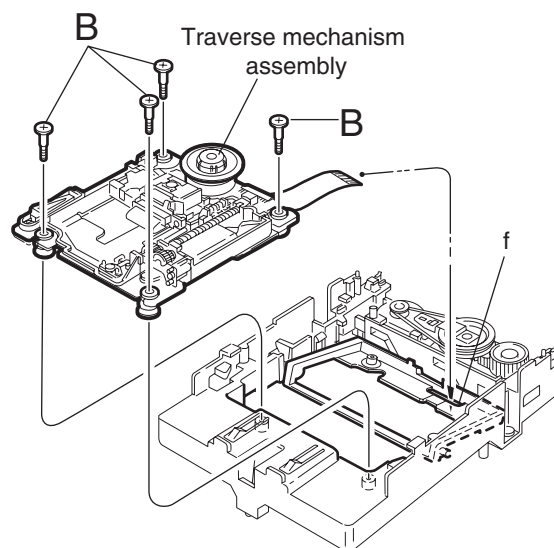
Fig.6
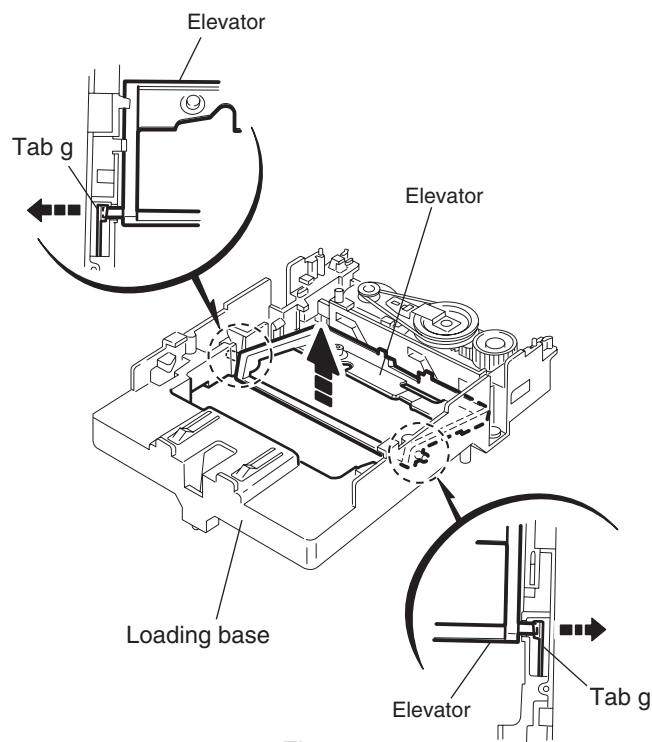
Fig.7
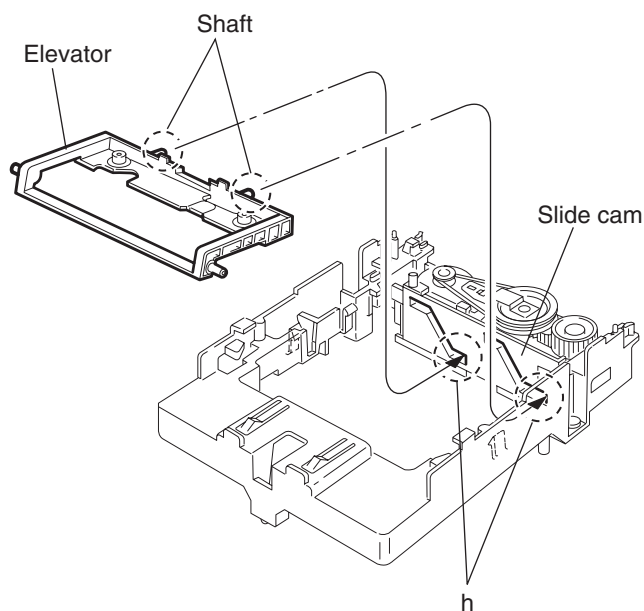
Fig.8

■Removing the motor assembly
(See Fig.9,10)

・ Prior to performing the following procedure, remove the clamper assembly, the tray, the servo control board, the traverse mechanism assembly and the elevator.

1. Remove the belt from the pulley.

2. Remove the screw **C** attaching the loading motor.

3. Remove the screw **D** attaching the motor board on the back of the loading assembly.

4. Release the tab **i** fixing the motor board and remove the motor assembly.

Belt

C

Loading motor pulley

Fig.9

Tab i

Motor board   D

Motor assembly   Loading assembly

Fig.10

Pulley gear bracket E

Pulley gear bracket

E

Idle gear

Idle gear

Tab j

Pulley gear

Pulley gear
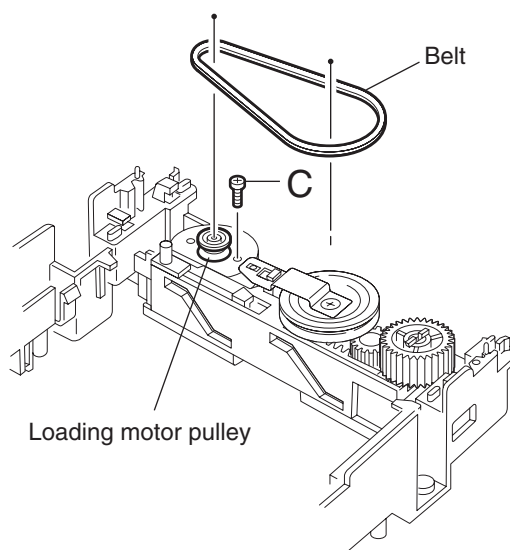
Pulley gear
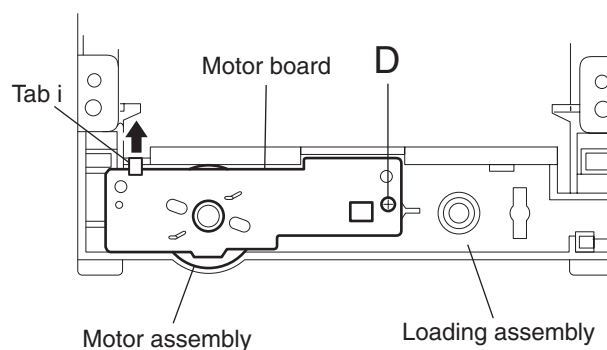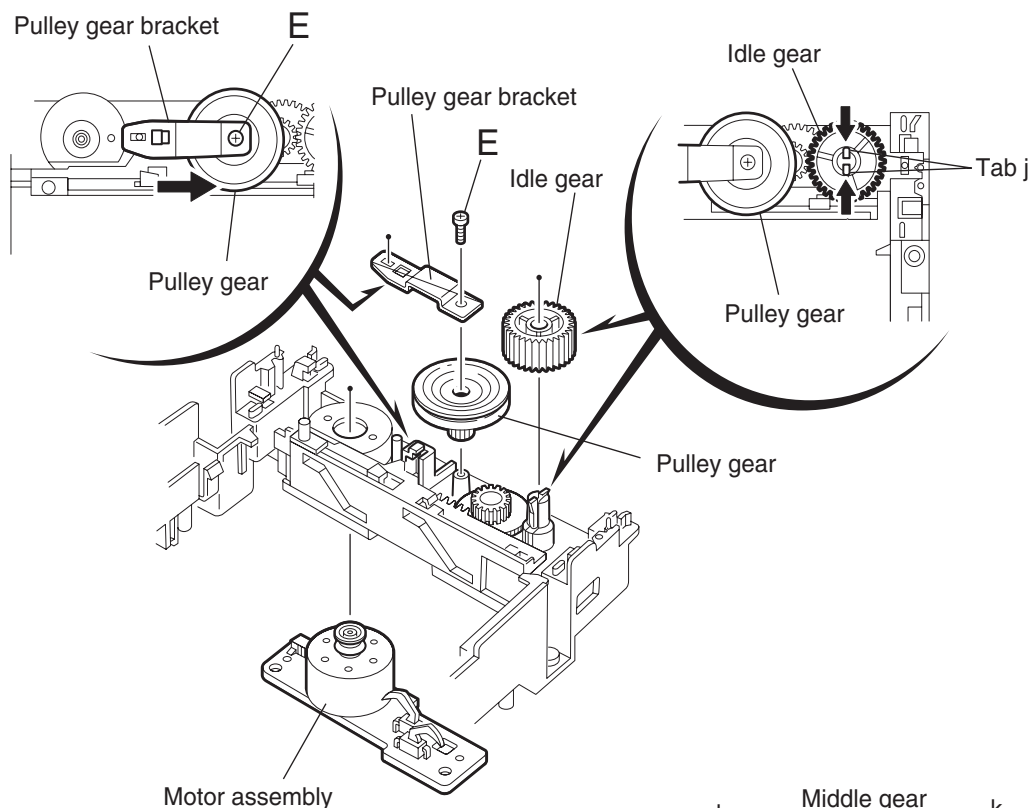
Motor assembly

Fig.11

■Removing the idle gear/ pulley gear/ middle gear/ slide cam   (See Fig.11~13)

・ Prior to performing the following the procedures, remove the clamper assembly, the tray, the servo control board, the traverse mechanism assembly, the elevator and the motor assembly.

1. Push the two tabs j attaching the idle gear inward and pull out the idle gear.

2. Remove the screw E attaching the pulley gear bracket. Move the pulley gear bracket in the direction of the arrow and remove upward.

3. Pull out the pulley gear.

4. Move the slide cam in the direction of the arrow to release the two joints k and remove upward.

5. Remove the middle gear.

k   Middle gear   k

Slide cam

Fig.12

Slide cam

Middle gear

Loading base
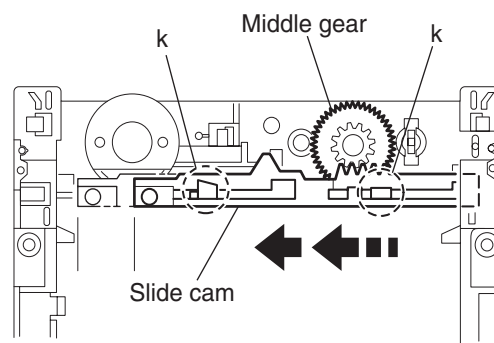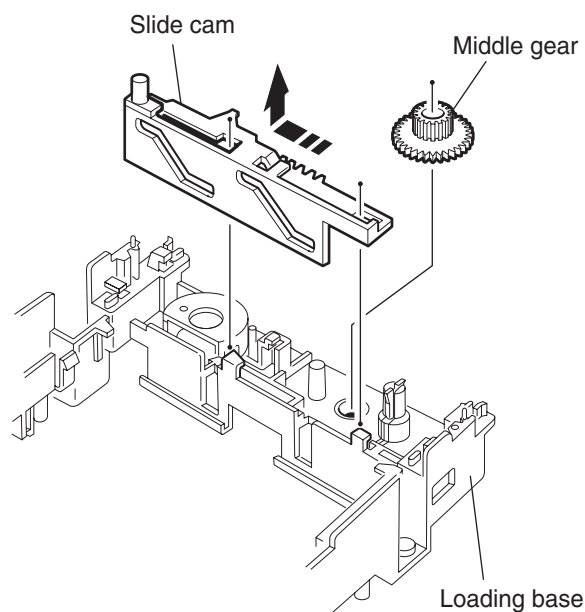
Fig.13

<DVD traverse mechanism assembly>

■Removing the feed motor assembly
(See Fig.14)

1. Unsolder the two soldering **I** on the spindle motor board.

2. Remove the two screws **F** attaching the feed motor assembly.
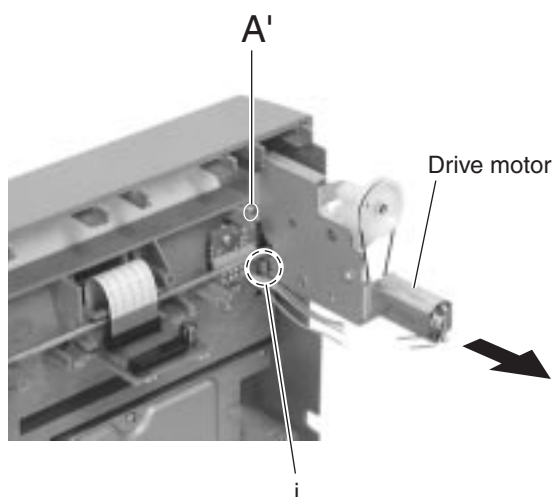
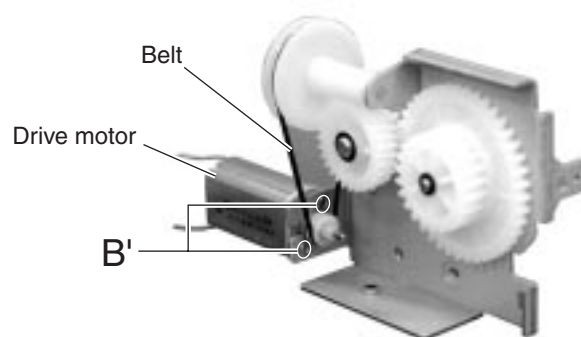### ■Removing the feed motor
(See Fig.14~16)

・ Prior to performing the following procedure, remove the feed motor assembly.

1. Remove the screw **G** and the spring.

> CAUTION: When reassembling, attach the spring correctly to press the feed gear M and E.

2. Remove the feed gear M.

3. Pull out the feed gear E and the lead screw.

4. Remove the two screws **H** and the feed motor.

> CAUTION: When reassembling, set the two wires extending from the feed motor to the notch **m** of the feed holder as shown in Fig.14.

Feed motor assembly

Pickup

Spindle motor

Spindle motor board

Fig.14

Feed gear M

Spring

Lead screw

Feed gear E
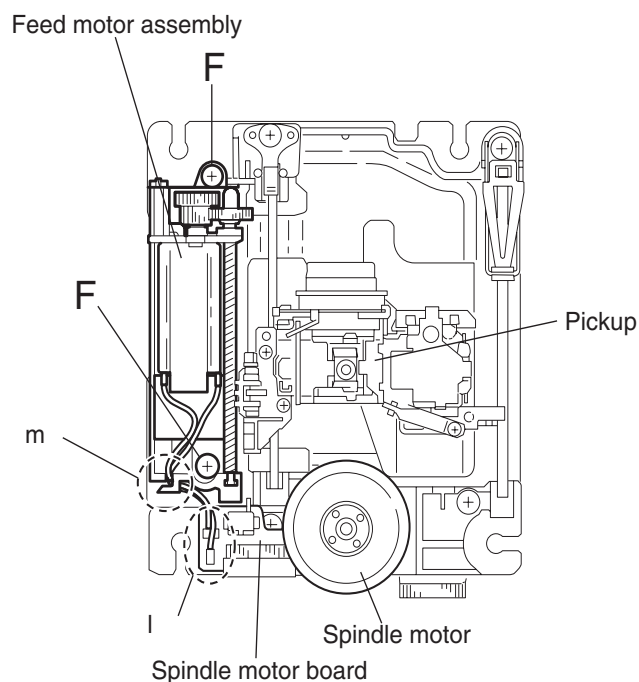
Fig.15
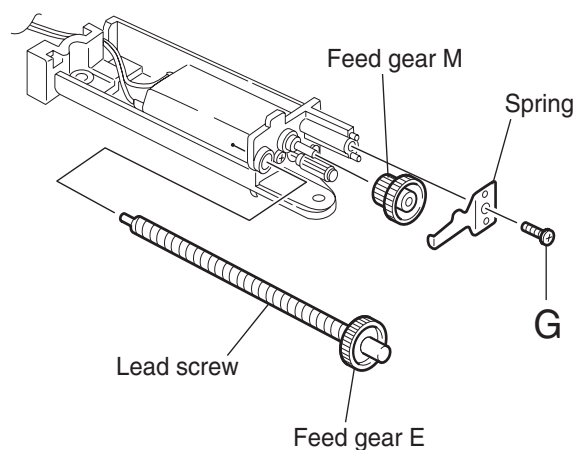
Feed motor
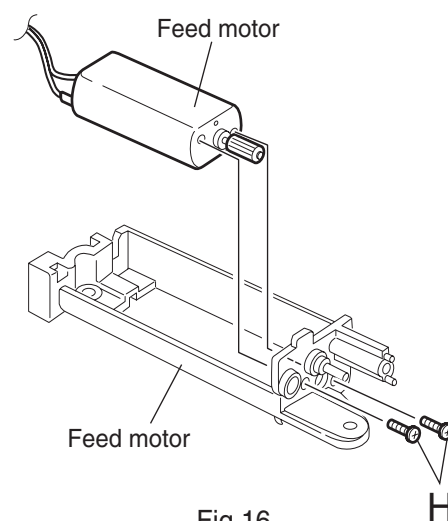
Feed motor

Fig.16

■Removing the pickup　　(See Fig.17,18)

1. Prior to performing the following procedure, remove the feed motor assembly.

2. Remove the screw **I**, the T spring(S) and the shaft holder with the plate.

> ATTENTION: When reassembling, reattach the T spring (s) correctly to press the shaft

3. Detach the part **n** of the shaft upward and move the part **o** in the direction of the arrow, then remove the shaft from the spindle base.

4. Release the joint **p** in the direction of the arrow.

   Pull out the shaft from the pickup.

5. Remove the two screws **J** attaching the actuator.

6. Release the joint of the actuator and the lead spring, and pull out the lead spring.

> ATTENTION: When reattaching the pickup, attach the spring under the shaft(See the figure below).

Spring　　Shaft　　Pickup
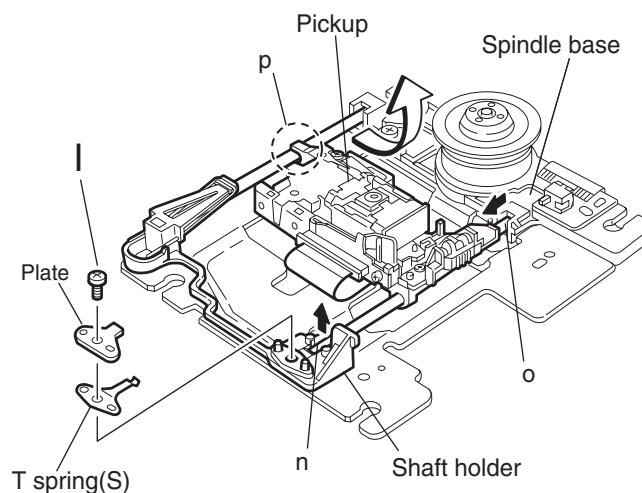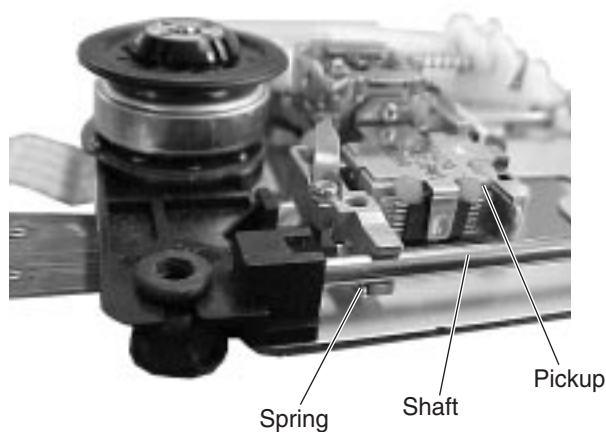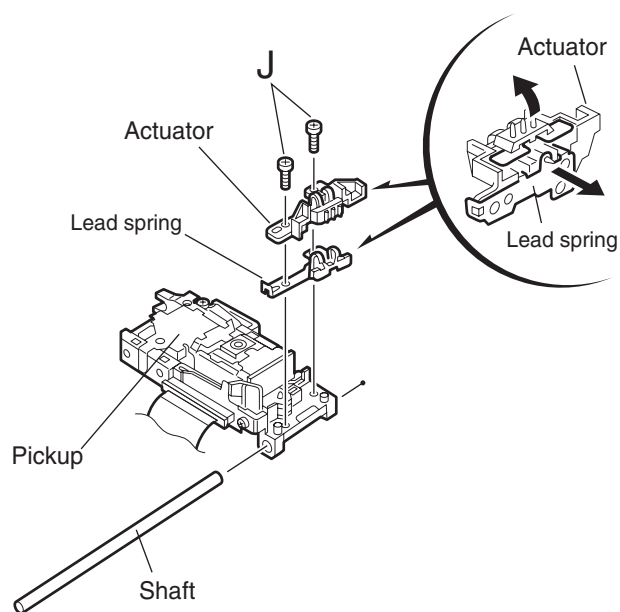
■Removing the shaft holder/ shaft (SeeFig.19)

・ Prior to performing the following procedure, remove the feed motor assembly and the pickup.

1. Remove the screw **K** attaching the shaft holder.

2. Remove the shaft.

Pickup　Spindle base
p
I
Plate
T spring(S)　　　n　　Shaft holder
o
Fig.17

Actuator
J
Actuator
Lead spring
Lead spring
Pickup
Shaft
Fig.18
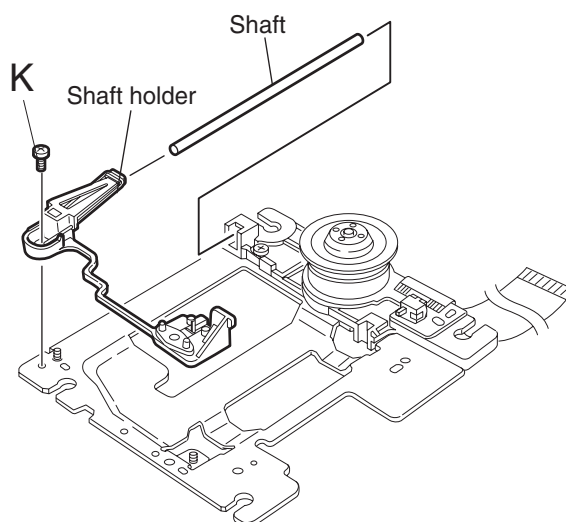
Shaft
K　　Shaft holder
Fig.19

■Removing the spindle motor assembly
(See Fig.20~22)

・ Prior to performing the following procedure, remove the feed motor assembly, the pickup, the shaft and the shaft holder.

1. Turn over the mechanism base and remove the three screws **L** attaching the spindle motor assembly.

> ATTENTION: When reassembling, set the card wire extending from the spindle motor board to the notch of the spindle base.

2. Remove the three screws **M** and the spindle base.

Spindle motor
L
L

Fig.20

Spindle motor assembly
Spindle motor board
Spindle base
L

Fig.21

M
M
Spindle base
Mechanism base
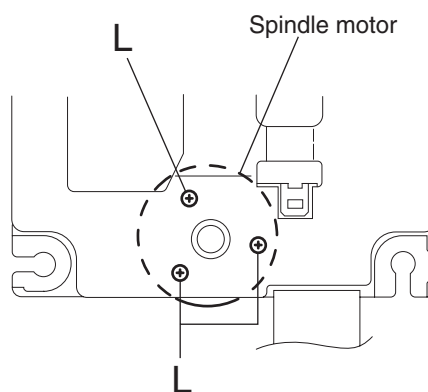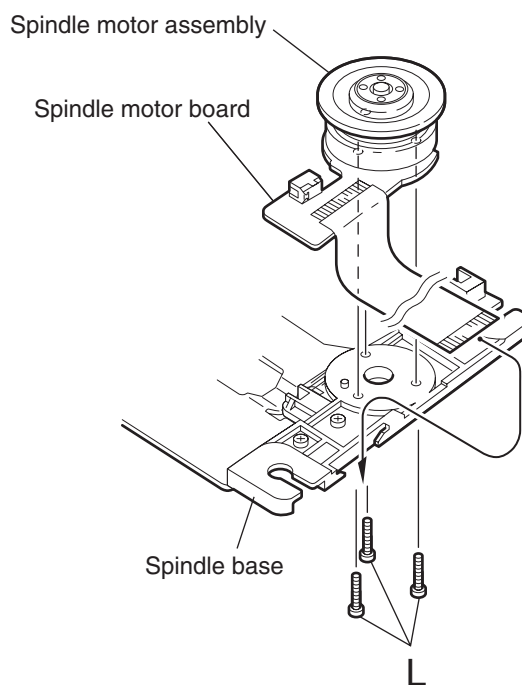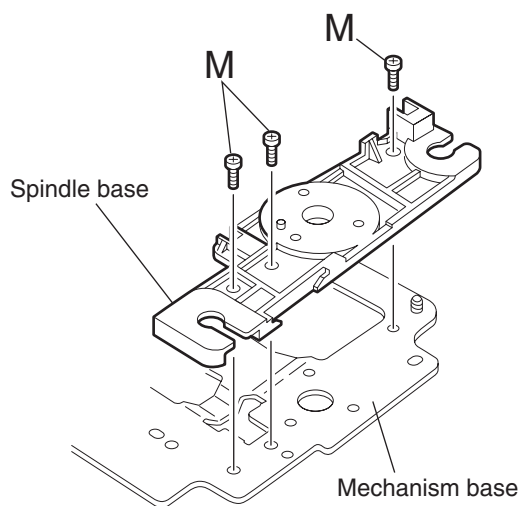
Fig.22

<MD mechanism assembly>

■Removing the main board (See Fig.1, 2)

> CAUTION: When replacing the flexible wire connected to the main board, solder the shorting round point. Otherwise, the pickup may be damaged. (see Fig.18)

1. Turn over the main body and disconnect the card wire from connector CN408 and the flexible wire from CN407 on the main board respectively.

2. Remove the two screws **A** attaching the main board. Move the main board in the direction of the arrow to release the two joints **a** .

3. Solder the sorting round point to protect the pickup. Disconnect the flexible wire from connector CN321 on the back of the main board.

> CAUTION: When reassembling, connect the flexible wire from the pickup to the main board and unsolder the shorting round point.

Main board

CN408

CN407

Joint a   Joint a

Fig.1

Main board

C451

CN321

Flexible wire

Pickup

Fig.2   Sorting round point
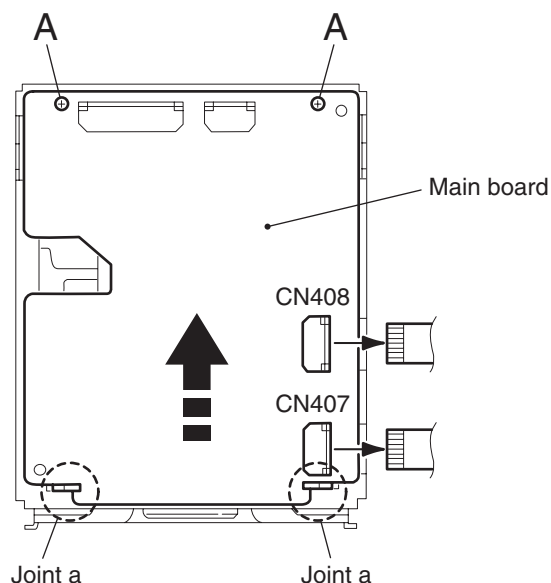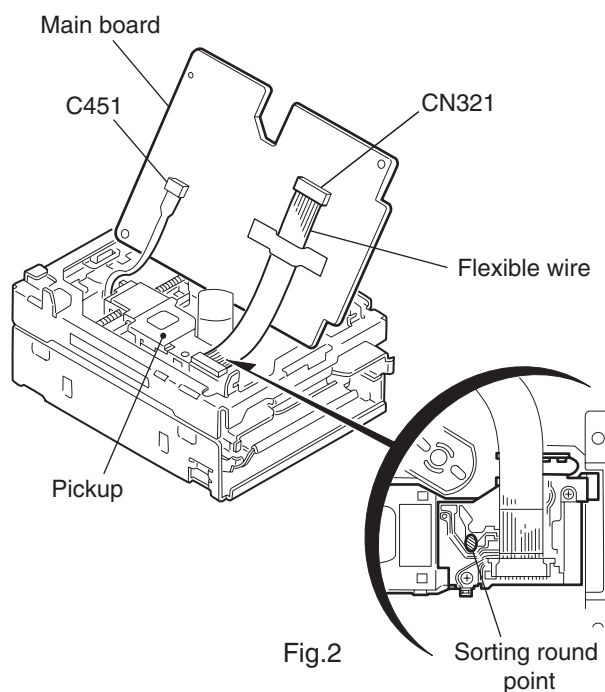
■Removing the mechanism cover (See Fig.3)

1. Remove the four screws **B** on each side of the body.

2. Remove the one screw **C** on the upper side of the body.

3. Move the mechanism cover toward the front to release the front hook from the loading assembly (joint **b**) , then remove upward.

C

Joint b

B

Hook

Mechanism cover

Joint c

B
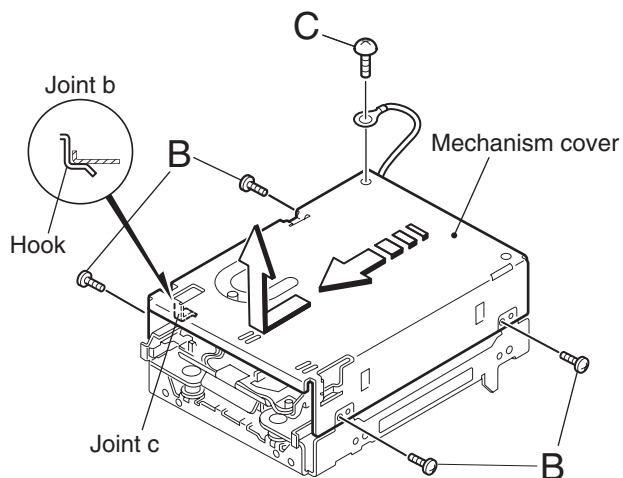
Fig.3

■Removing the head lifter   (See Fig.4~6)

1. Removing the spring from the hook on the main body. Remove the spring from the head lifter if necessary.

2. Turn the head lifter in the direction of the arrow to release the joint **c** and **d** .

Head lifter

Fig.4

Joint c

Head lifter   Joint d

Spring

Fig.5

Head lifter

Spring

Fig.6
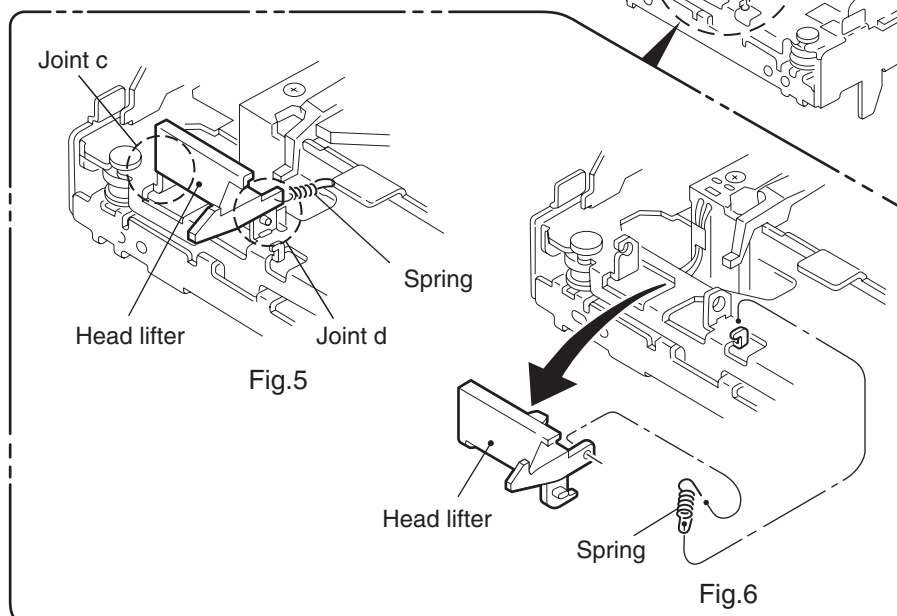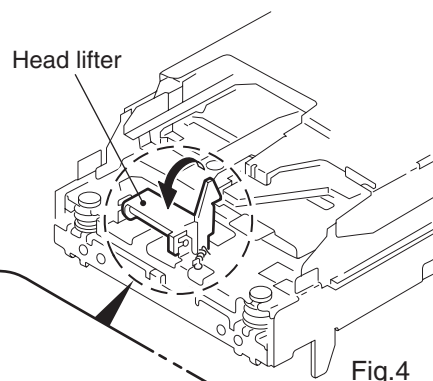
■Removing the head assembly (See Fig.7)

・ Prior to performing the following procedure, remove the main board.

1. Remove the screw **D** on the upper side of the body. Remove the head assembly while pulling the flexible harness from the body.

Head assembly

D

Fig.7
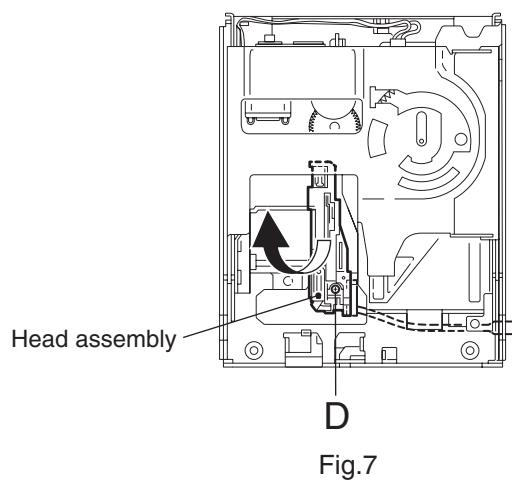
■Removing the loading assembly
(See Fig.8, 9)

REFERENCE: The traverse mechanism assembly and the single flame can be removed after removing the loading assembly from the body.

・ Prior to performing the following procedure, remove the main board, the mechanism cover and the head lifter/head assembly.

1. Remove the three screws **E** on the upper side of the body.

2. Move the loading assembly toward the front to release the joint **e** and remove upward.

3. Remove the traverse mechanism assembly from the single flame.

E   E

Loading assembly

Joint e

E

Fig.8

Loading assembly

Traverse mechanism assembly

Single frame
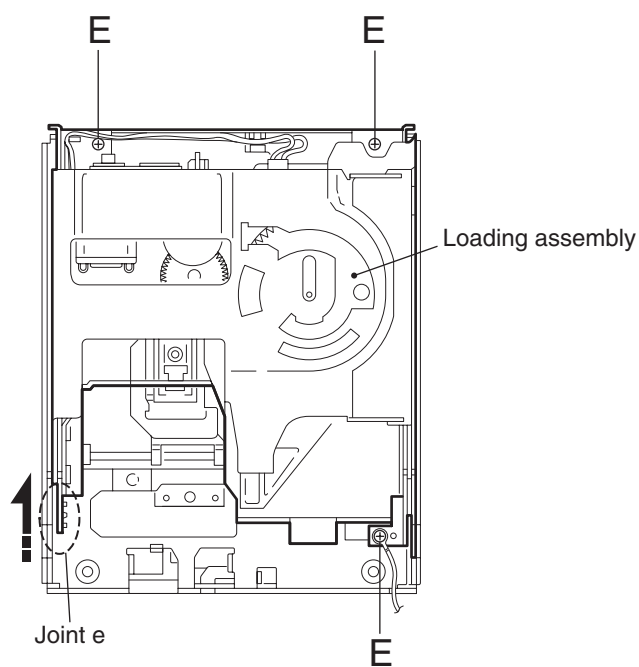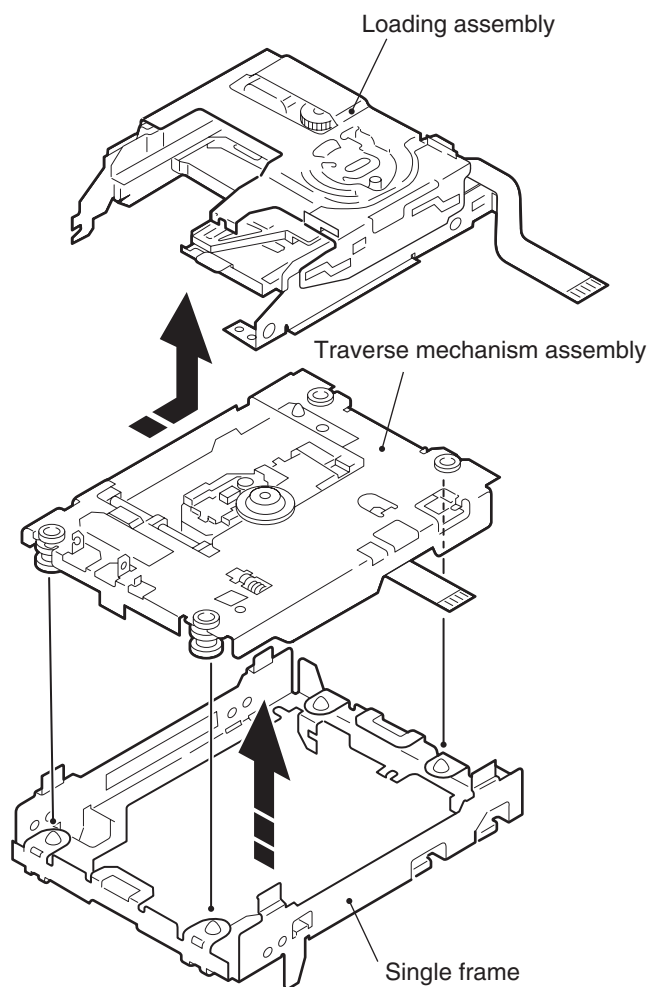
Fig.9

<Loading assembly section>

■Removing the slide base (L) and (R)
(See Fig.10)

1. Remove the two screws **F** on the upper side of the loading base assembly.

2. Remove the slide base (L) outward while releasing the two joints **f** on the bottom.

3. Remove the slide base (R) outward.
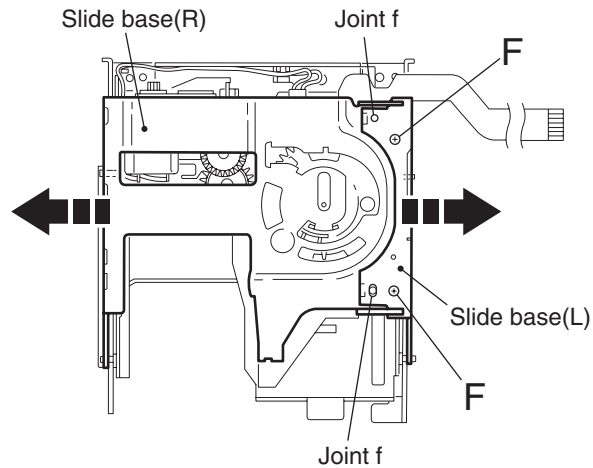
Fig.10

■Removing the loading mechanism assembly
(See Fig.11)

1. To release the loading mechanism assembly from the bending **g** without trouble, first bring up the one side of the loading mechanism assembly opposite to the bending **g** and release the side bosses from the loading mechanism base. And next, remove another side.
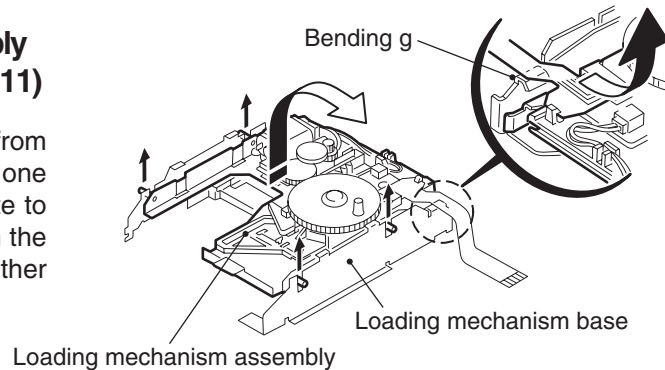
Fig.11

— Loading mechanism assembly section —

■Removing the loading motor
(See Fig.12, 13)

1. Release the harness from the wire holder on the cam switch board and disconnect from connector t.

2. Remove the screw **G** and release the joint **h**.

3. Remove the belt from the loading motor assembly.

4. Remove the two screws **H**.
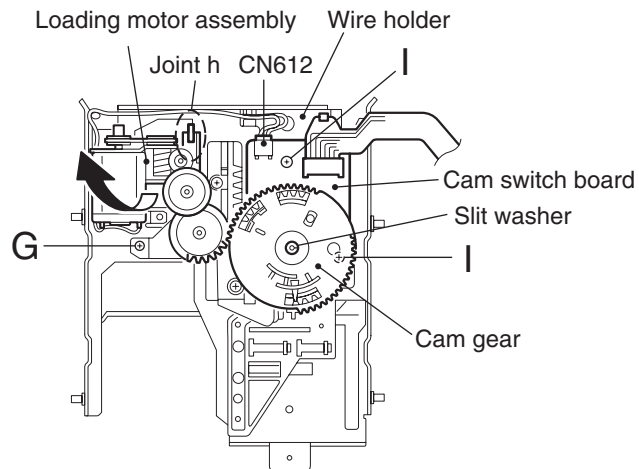
Fig.12

■Remove the cam gear and the cam switch board
(See Fig.12)

1. Remove the slit washer and pull out the cam gear.

2. Release the harness from the wire holder on the cam switch board and disconnect from connector CN612.

3. Remove the two screws **I**, the clamp and the cam switch board.
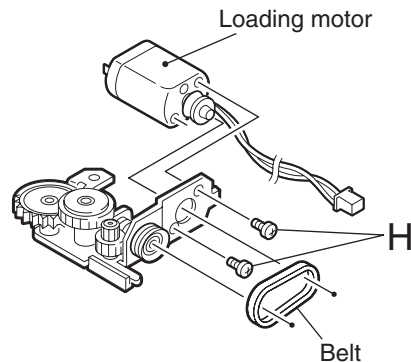
Fig.13

■Remove the cartridge holder assembly (See Fig.14, 15)

1. Remove the two screws **J** on the upper side of the loading assembly.
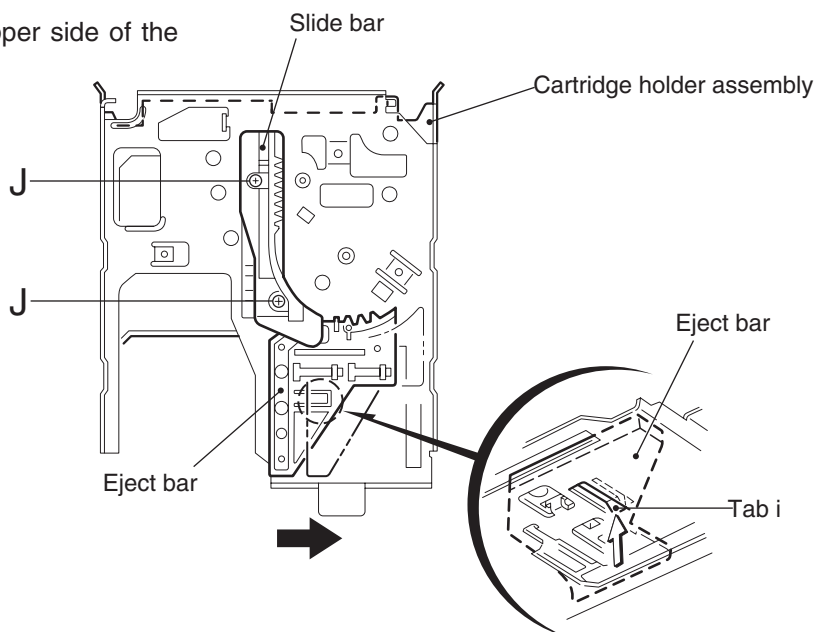
Fig.14

■Removing the slide bar/Eject bar (See Fig.14, 15)

・ Prior to performing the following procedure, remove the cartridge holder assembly.

1. Remove the slide bar upward.

2. Move the slide bar outward until it stops (See Fig.14). Push the tab **i** from below and remove the eject bar from the chassis section.

Fig.15

<Traverse mechanism assembly section>

■Removing the insulator   (See Fig.16)

1. Removing the insulators from the four notches of the traverse mechanism chassis.
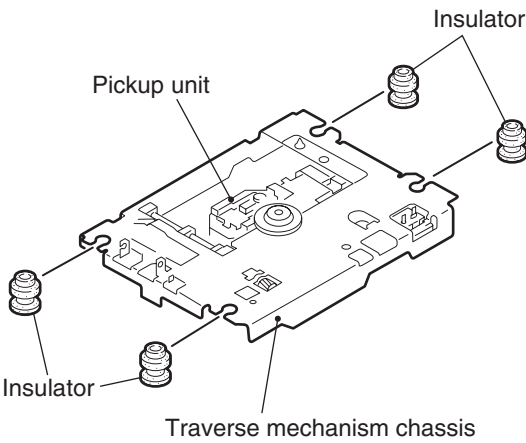
Fig.16

■Removing the pickup unit   (See Fig.17)

1. Remove the screw **K** attaching the shaft holder (F) on the back of the traverse mechanism assembly.

2. Move the shaft inward and release from the shaft holder (R).

3. Bring up the one side of the pickup unit on the shaft to release the joint **j** on the opposite side. Then, remove the pickup unit with the shaft.
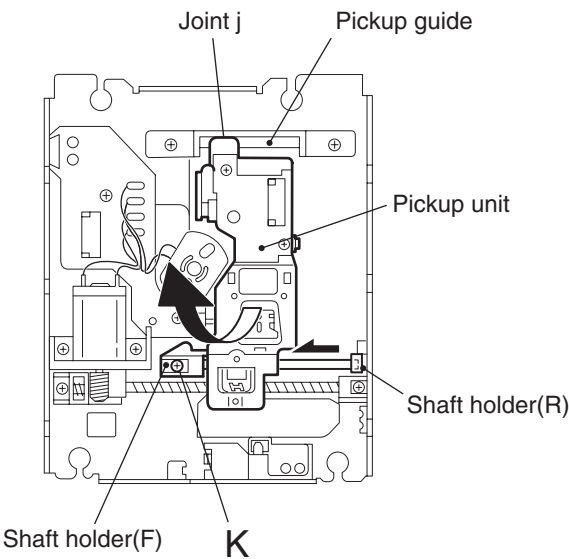
Fig.17

■Removing the pickup   (See Fig.18)

1. Pull out the shaft from the pickup.

2. Remove the two screws **L** attaching the rack spring to the pickup.

CAUTION: Before disconnecting the flexible wire connected to the pickup, solder the shorting round point to protect the pickup from static electricity.
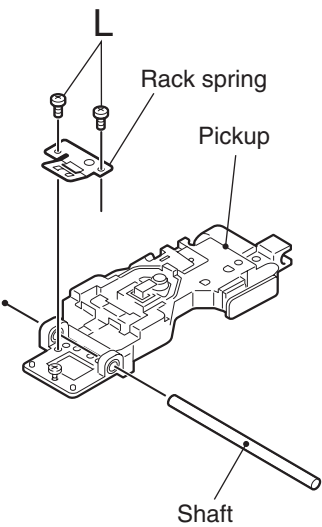
Fig.18

■Removing the feed motor assembly
(See Fig.19,20)

REFERENCE: The feed motor assembly can be performed even if the pickup unit is attached.

1. For the white and black harnesses extending from the feed motor assembly, unsolder two soldering **k** on the traverse mechanism board.

2. Remove the two screws **M** attaching the feed motor assembly.

3. Remove the two screws **O** attaching the feed motor bracket.
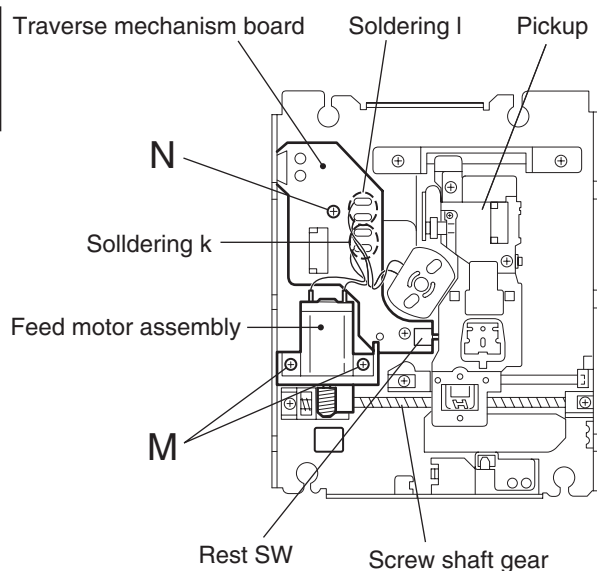
■Removing the traverse mechanism
board (See Fig.19)

・ Prior to performing the following procedure, remove the feed motor assembly.

1. For the red and black harnesses extending from the spindle motor, unsolder two soldering **l** on the traverse mechanism board.

2. Remove the screw **N**.

CAUTION: When reattaching the traverse mechanism board, make sure the position of the pickup. If the pickup is on the most inside position, move it outward by turning the screw shaft gear not to contact with the rest SW.

Traverse mechanism board   Soldering l   Pickup

N

Solldering k

Feed motor assembly

M

Rest SW   Screw shaft gear

Fig.19

Feed motor

Feed motor bracket

O

Fig.20

UX-A10DVD

<Reattaching the loading
assembly section>
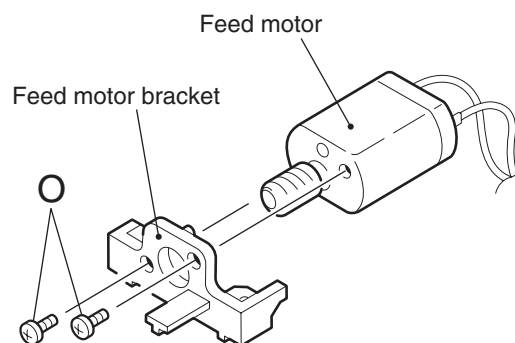
1. Reattach the eject bar to the UD base (see Fig.15, 21).

2. Reattach the slide bar to the loading mechanism chassis while fitting the boss **m** to the groove of the eject bar (see Fig.15).

3. Move the slide bar and eject bar in the direction of the arrow and reattach the cartridge holder assembly using the two screw **J** (Fig.21, 22).

CAUTION: Make sure that pin **n** of the eject bar is correctly fitted in the groove **o** when moving the eject bar and the loading slider as shown in Fig.22.

Wire holder

Cam switch board

p

q

Mark

Slide bar

J

J

Cam switch boss

Groove

UD base

Eject bar

Fig.21

UD base(Bottom)

Cartridge holder assembly

Groove o

Loading slider

Eject bar

Pin n
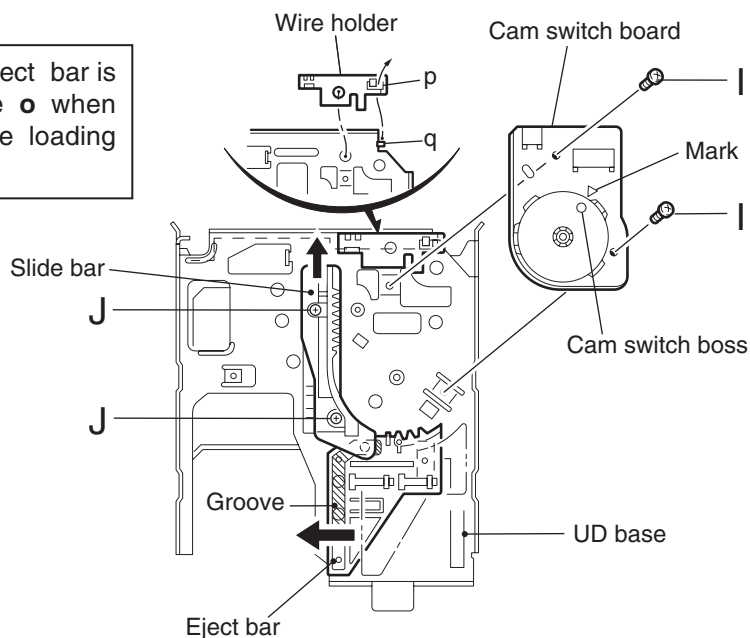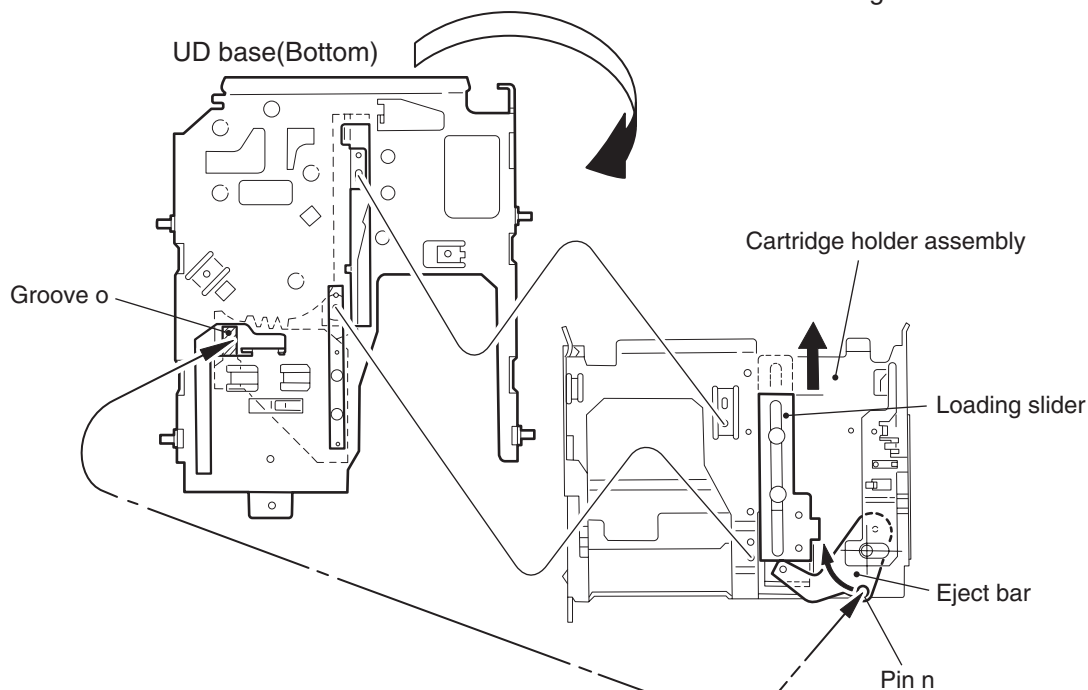
Fig.22

4. Reattach the wire holder to the UD base while fitting the bending **q** to the hole of the wire holder (The boss on the back of the wire holder is fit to the hole of the UD base)(see Fig.21).

5. Reattach the cam switch board using the two screws **I** .

6. Turn the cam switch until the boss comes to the position marked with a triangle (see Fig.23). Reattach the cam gear while fitting the cam gear slot to the cam switch boss, and fix them using the slit washer.

> CAUTION: When reattaching the cam gear with fitting the slot to the cam switch boss, make sure that part **r** of the gear is aligned with the position marked with a triangle of the cam gear.

7. Reattach the loading motor assembly using the screw **G** (see Fig.23).

Connect the wire extending from the loading motor to connector CN612 on the switch board, set on the bending **s** of the UD base and fix using the wire holder.
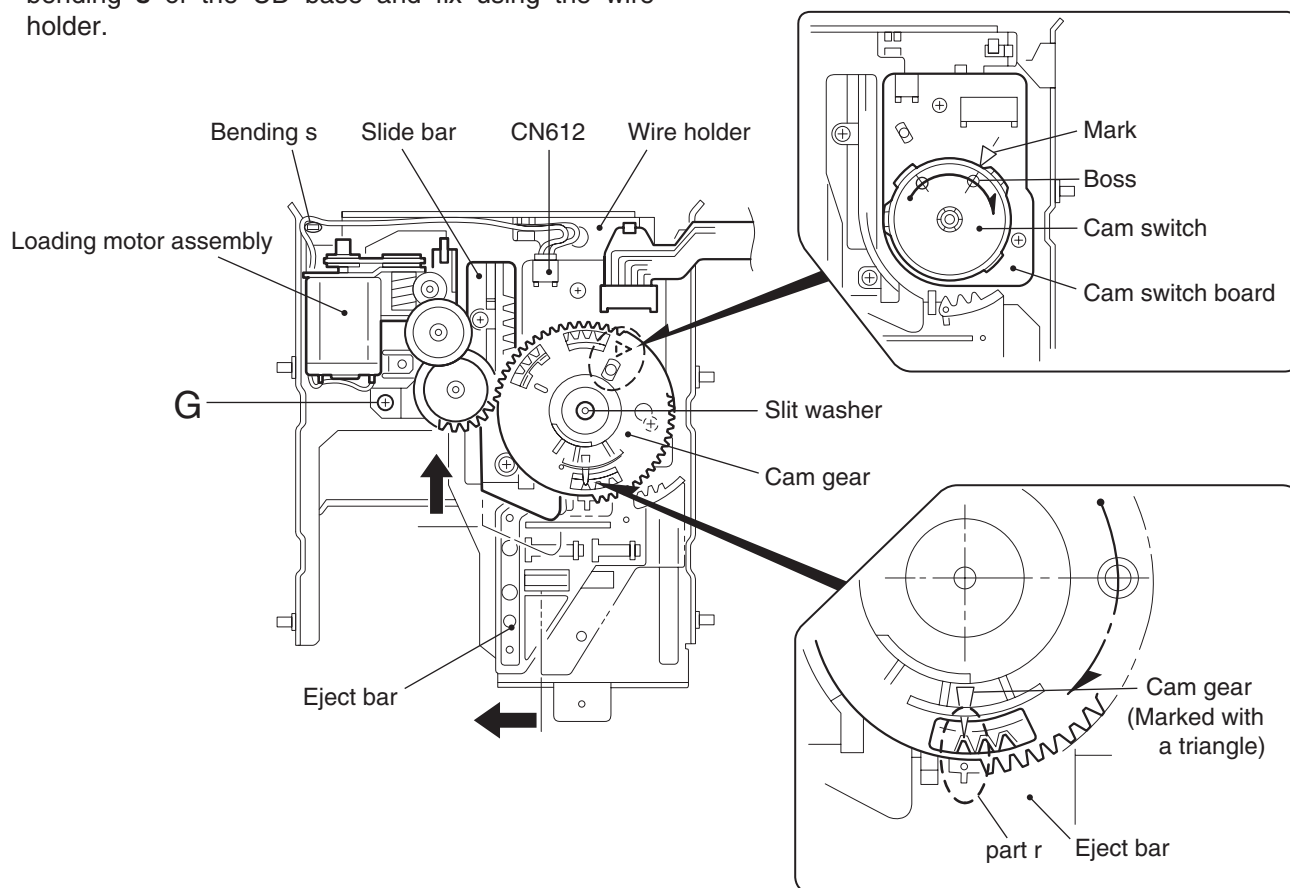
Fig.23

8. Reattach the UD base to the loading mechanism base while fitting the four bosses to the notches of the loading mechanism base respectively (see Fig.24).

   First, sit part **t** of the cartridge holder assembly under the bending **g** of the loading mechanism base, then reattach the UD base.

9. Reattach the slide base (R) while fitting the two slots of the slide base (R) to the bosses of the UD base (see Fig.25, 26).

   CAUTION: Set the bending **u** of the slide base (R) to the part **v** inside of the cam gear rib.

10. Reattach the slide base (L) on the slide base (R) while fitting the two bosses of the UD base to the notches on the side of the slide base (L). Make sure that the slots of the slide base (L) are fitted to the two part **f** and fix the slide base (L) using the two screws **F** (see Fig.25, 27).

   REFERENCE: To reattach the slide base (L) and (R) easily, fit the bosses to the notches with bringing up the UD base slightly.
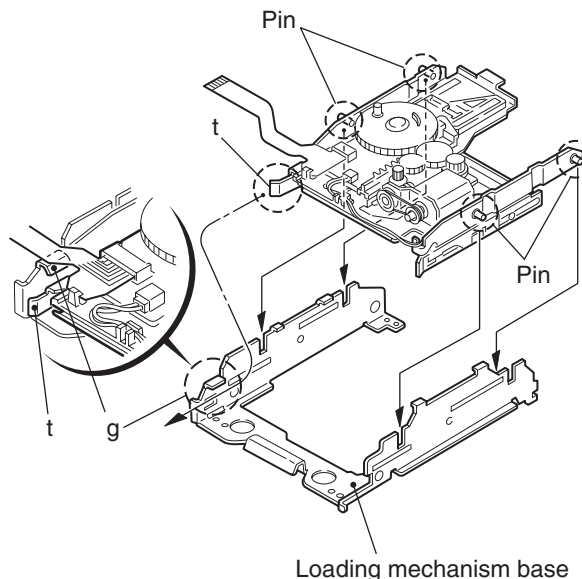
Fig.24
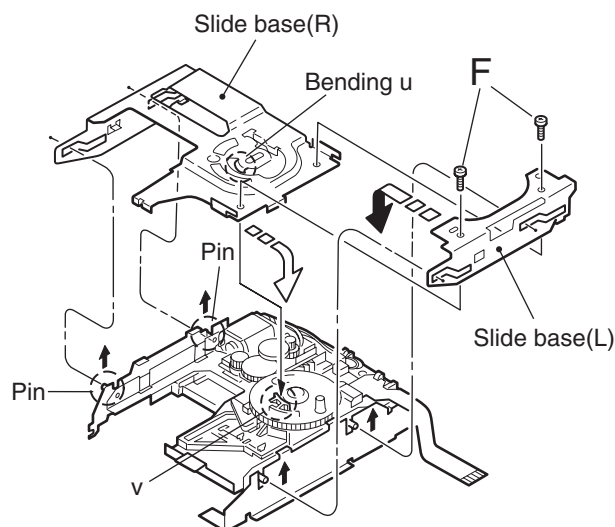
Fig.25
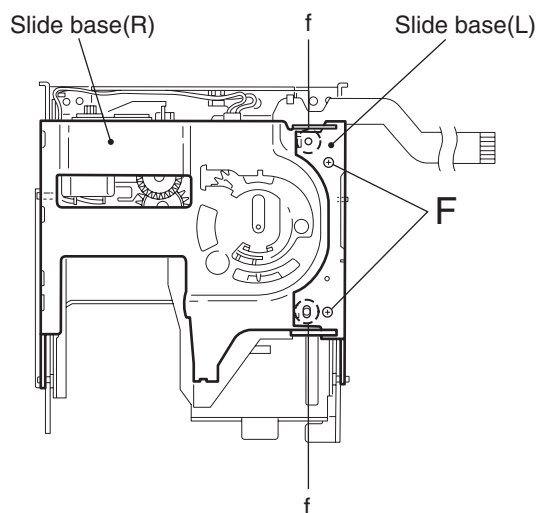
Fig.27
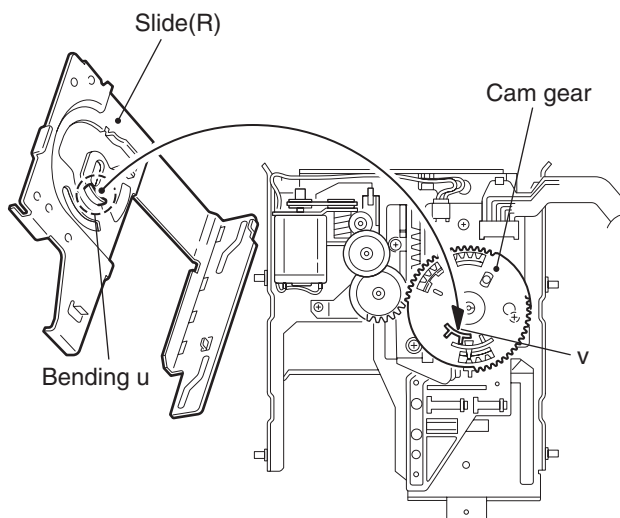
Fig.26

<Cassette mechanism assembly section>

■Removing the Play/Record & Clear head
(See Fig.1~3)

1. While moving the trigger arm on the right side of the head mount in the direction of the arrow, turn the flywheel R counterclockwise until the head mount comes ahead and clicks.

2. The head turns counterclockwise as you turn the flywheel R counterclockwise(See Fig.2 and 3).

3. Disconnect the flexible wire from connector CN31 on the head amplifier & mecha control board.

4. Remove the spring from the back of the head.

5. Loosen the azimuth screw for reversing attaching the head.

6. Remove the head on the front side of the head mount.

Cassette mechanism assembly   Fly wheelR

Head mount   Trigger arm

Fig.1

Head

Fly wheel R

Fig.2

Azimuth screw
for reversing

Head

Flexible wire

Spring

CN31
Head amplifer & mecha control board

Fig.3

1-35
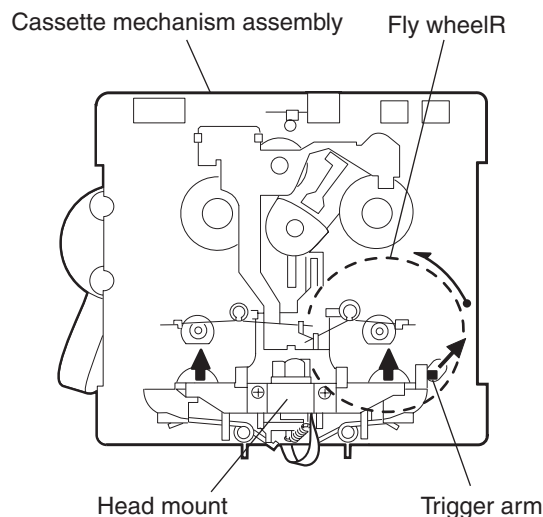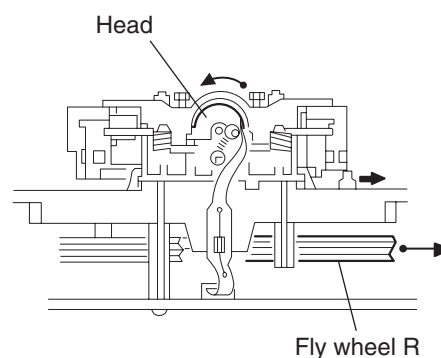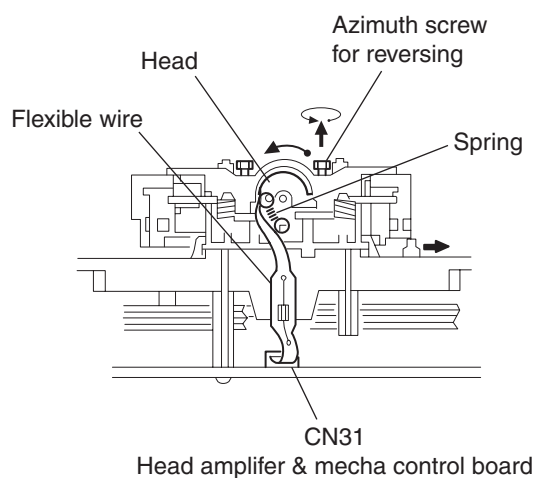
■Removing the head amplifier & mechanism control board (See Fig.4)

1. Turn over the cassette mechanism assembly and remove the three screws **A** attaching the head amplifier & mechanism control board.

2. Disconnect the flexible wire from connector CN31 on the head amplifier & mechanism control board.

3. Disconnect connector CN32 of the head amplifier & mechanism control board from connector CN1 on the reel pulse board.

REFERENCE: If necessary, unsolder the 4 pin wire soldered to the main motor.

Head amplifier & mecha control board

A   CN32

CN31

A

Flexible wire   4pin wire

B

Main motor assembly
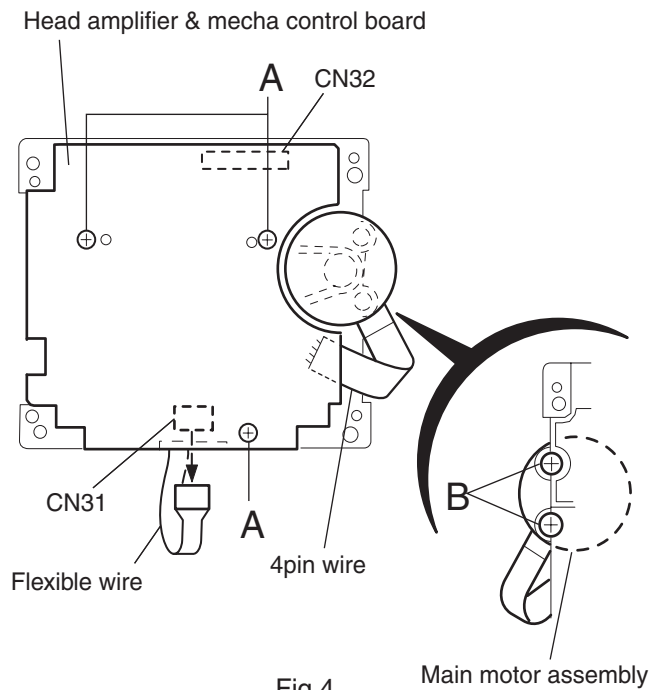
Fig.4

■Removing the main motor (See Fig.4~7)

1. Remove the two screws **B** .

2. Half raise the motor and remove the capstan belt from the motor pulley.

ATTENTION: Be careful to keep the capstan belt from grease. When reassembling, refer to Fig.6 and 7 for attaching the capstan belt.

Main motor assembly

Capstan belt

Fig.5

Main motor assembly

Capstan belt

Motor pulley

Fig.6

Main motor assembly

Fly wheel

Capstan belt   Motor pulley
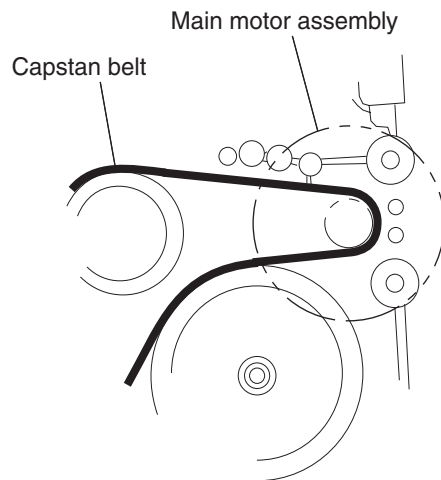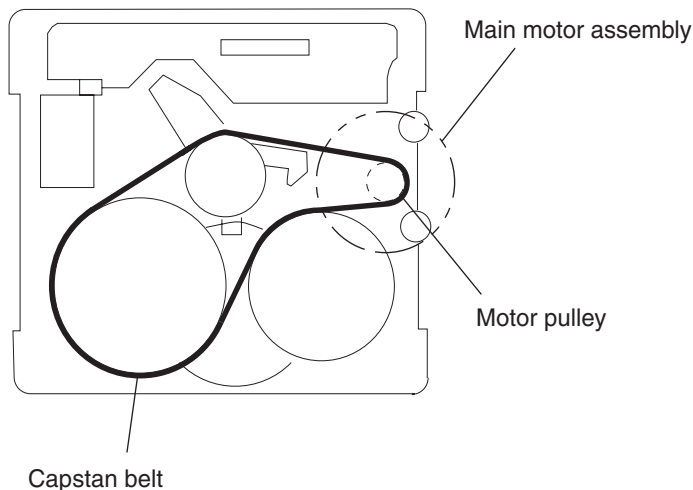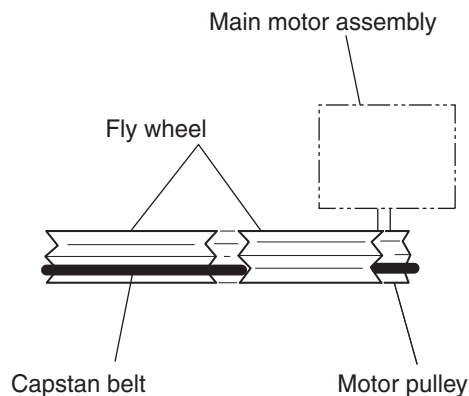
Fig.7

■Removing the flywheel　　(See Fig.8,9)

・ Prior to performing the following procedure, remove the head amplifier & mechanism control board and the main motor assembly.

1. From the front side of the cassette mechanism, remove the slit washers attaching the capstan shaft L and R. Pull out the flywheels backward.

Fly wheel R　　　　　Fly wheel L

Fig.8

Fly wheel R　　　　　　　Fly wheel L

Capstan shaft R ———　　　　——— Capstan shaft L

Slit washer
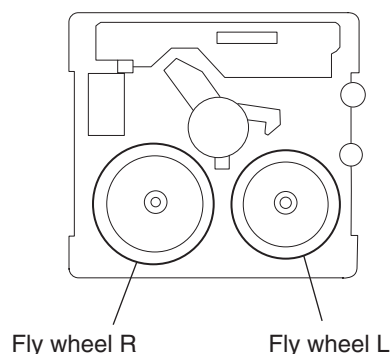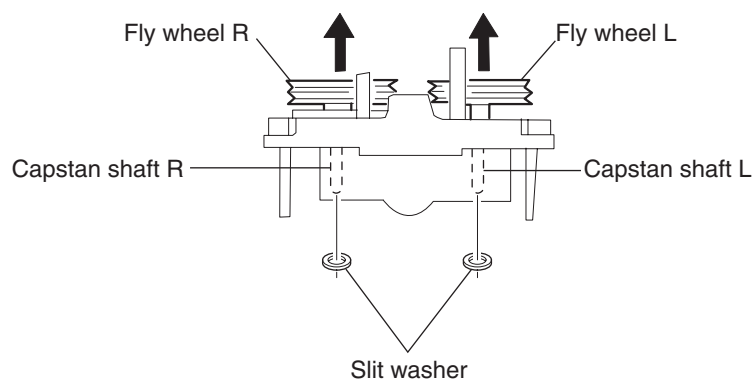
Fig.9

■Removing the reel pulse board and solenoid　　　(See Fig.10)

・ Prior to performing the following procedure, remove the head amplifier & mechanism control board.

1. Remove the screw **C**.

2. Release the tab **a**, **b**, **c**, **d** and **e** retaining the reel pulse board.

3. Release the tab **f** and **g** attaching the solenoid on the reel pulse board.

4. The reel pulse board and the solenoid come off.

a　　b　　c　　d　　Reel pulse board

Solenoid

f　g

C

e
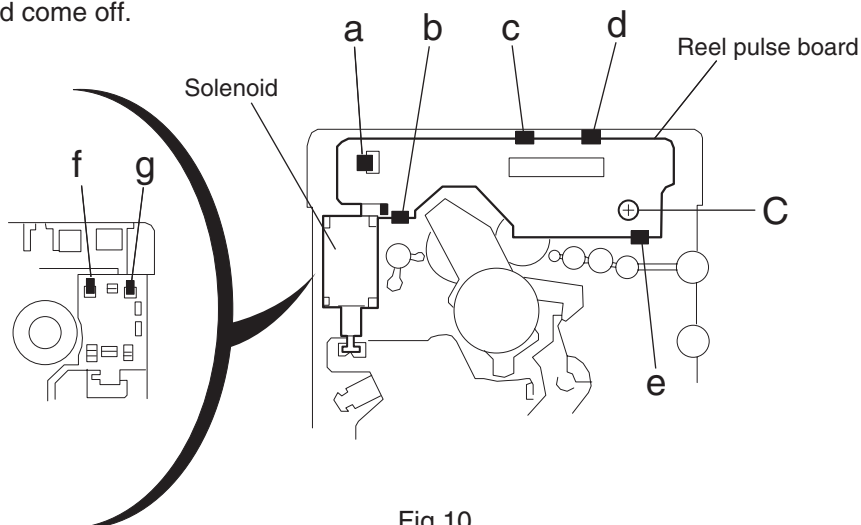
Fig.10

■Reattaching the Play/ Record & Clear head (See Fig.11~13)

1. Reattaching the head mount assembly.

   1) Change front of the direction cover of the head mount assembly to the left(Turn the head forward).

   2) Fit the bosses **O'**,**P'**,**Q'**,**U'** and **V'** on the head mount assembly to the holes **P** and **V**, the slots **O**,**U** and **Q** of the mecha sub assembly(See Fig.11 to 13).

   > CAUTION: To remove the head mount assembly, turn the direction cover to the left to disengage the gear. If the gear can not be disengaged easily, push up the boss **Q'** slightly and raise the rear side of the head mounts slightly to return the direction lever to the reversing side.

2. Tighten the azimuth screw for reversing.

3. Reattach the spring from the back of the Play/ Record & Clear head.

4. Connect the flexible wire to connector CN31 on the head amplifier & mechanism control board.
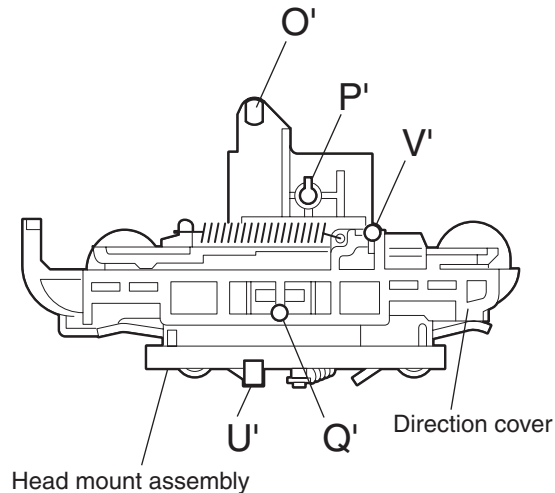
Fig.11
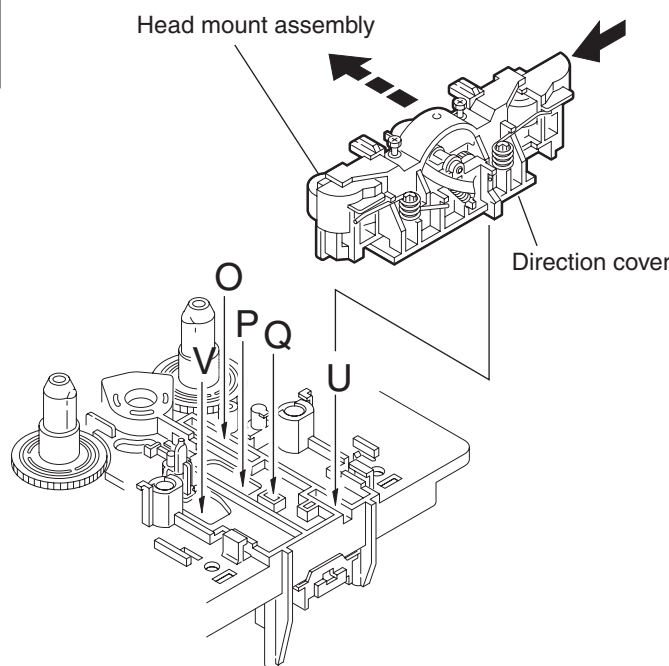
Fig.12
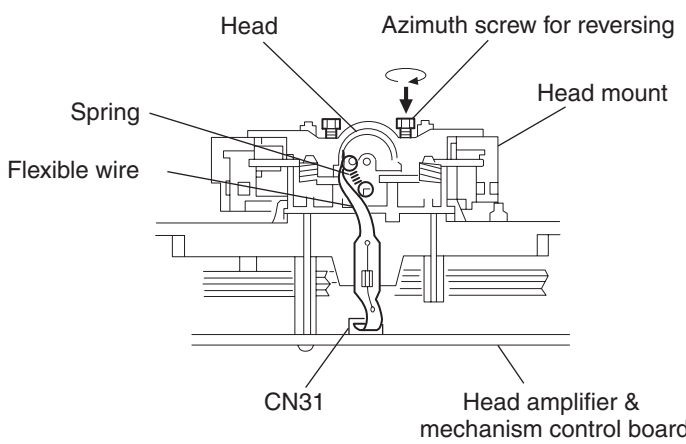
Fig.13

Adjustment method

< MD adjustment (self adjustment) >

(1) Setting of adjustment mode of MD

```
While pressing both the POWER
key and REC key, turn on the
primary power supply.
```
↓
```
FL indication
TEST MODE 1
```
↓
```
STOP key of the main body pushed
for stopped MD  after power supply
ON with  pushed the MD PLAY key.
```
↓
```
FL indication
TEST MODE 1
```
↓
```
Setup is complete.
```

(3) Adjustment of the playback laser power

```
Changes to the adjustment
mode of MD.
```
↓
```
Insert the laser power
meter sensor.
```
↓
```
Press the "2" key on
the remote controller.
```
↓
```
Set up the playback
laser power.
```
↓

| Increase the laser power with the F. SKIP key on the remote controller. | Decrease the laser power with the B. SKIP key on the remote controller. |

↓
```
Adjust the power to be 0.68 mW or
more. If the value exceeds 0.68 mW,
approximate it to 0.68 mW as
accurately as possible.
```
↓
```
Press the STOP key
on the main unit.
```
↓
```
Setup of the MD laser
power is complete.
```

(2) Initialization of EEPROM
(The EEPROM can be initialized on the precondition that the setup of the TEST MODE 1 is complete. After setup of the TEST MODE 1, proceed to the following operations with the remote controller*.)
* For EJECT operation, use the EJECT key on the main unit.

```
changes to the adjustment
mode of MD.
```
↓
```
FL indication
TEST MODE 1
```
↓
```
Press the PLAY MODE key
on the remote controller.
```
↓
```
FL indication
TEST MODE 1
```
↓
```
Initialization completion
of EEPROM
```
↓
```
Four buttons of remote
control are pushed.
```
↓
```
Recording laser power setting
```
↓

| Increase the laser power with the F. SKIP key on the remote controller. | Decrease the laser power with the B. SKIP key on the remote controller. |

↓
```
It is adjusted with 6.23mW or less to
a value which is unlimited and close
to 6.23mW.
```
↓
```
Press the STOP key
on the main unit.
```
↓
```
EJECT does the sensor of the laser
power meter with the EJECT button
of the main body.
```
↓
```
Setup of the MD laser
power is complete.
```

UX-A10DVD

(4) Adjustment of the disk

Set up the TEST MODE 1.

Insert the premastered disk.

Reading of TOC ends.

Press the MD PLAY key on the remote controller.

FL indication ON TUNING

Automatic adjustment starts.

Adjustment OK? — NO

YES

FL indication OK TUNING

FL indication NG ERR: XX

Press the STOP key on the remote controller.

Press the EJECT key on the main unit.

Insert a recordable disk.

Press the MD PLAY key on the remote controller.

FL indication ON TUNING

Automatic adjustment starts.

Adjustment OK? — NO

YES

FL indication ON TUNING

FL indication NG ERR: XX

Press the STOP key on the remote controller.

Press the MD EJECT key on the main unit.

Automatic adjustment ends.

Press the POWER key on the main unit or remote controller.

Cut off the power supply after cancelling the TEST MODE.

NG Judgment Code Table

Code	NG item in adjustment
00	Automatic adjustment is incomplete.
01	Rest switch detection
02	Focus-on
03	EF balance, tracking offset adjustment (Pit area)
04	ABCD level (I-V resistance) adjustment (Pit area)
05	Focus servo AGC (Pit area)
06	Tracking servo AGC (Pit area)
07	Focus bias adjustment (Pit area)
08	EF balance, tracking offset adjustment (GRV area)
09	ABCD level (I-V resistance) adjustment (GRV area)
0A	Focus servo AGC (GRV area)
0B	Tracking servo AGC (GRV area)
0C	Focus bias adjustment (GRV area)
0D	Room temperature measurement
0E	Write in EEPROM
FF	Automatic adjustment is complete.

<Method of setting DVD test mode>

1. Main body "Stop button ■ " and "DVD eject button ▲ " are pushed at the same time, and the power supply is turned on.
2. The display of the FL display becomes "TEST D", and becomes a test mode.

T	E	S	T				D		R	2

3. Comes off the test mode when the power supply is turned off by "STANDBY button ⏻/I ".

4. Use key in test mode

      [STOP]+[DVD EJECT]+AC opening:Test mode
      [STANDBY]:Test mode release

      [ON SCREEN] : Self adjustment command for test
      [DVD EJECT] : EJECT command for test
      [STOP] : STOP command for test
      [DVD PAUSE] : Self adjustment command for test
      [DVD PLAY] : Jitter measurement command for test
      [ENTER] : EEPROM initialization command
      [▶▶I] : Outer tracking OFF command
      [I◀◀] : Tracking OFF of surroundings on inside command
      [1]~[9] : Servo relation examination command
      [MENU] : Display of number of ROM
      [TOP MENU] : Display of number of ROM

5. Content of processing

(1)   A reproduction and posed inside display the jitter measurement value and the value of the current of the laser on the FL display in the TEST mode.

        FIX4   BYTE7   Value of current of laser (subordinate position)
                    BYTE8   Value of current of laser (high rank)
                    BYTE9   Jitter measurement value (subordinate position)
                    BYTE10   Jitter measurement value (high rank)

FL display

T	E	S	T				D		R	2
	X	X	X	X			Y	Y	Y	Y

Value of current of laser	Jitter measurement value

• Value of current of laser

FL display(Example)

```
0033   0000
```
↑
Value of current of laser

Remote control "4" button Value of current of laser for CD
Remote control "5" button Value of current of laser for DVD

As for the value of the current of the laser, the figure displayed on the FL display
reaches the current value as it is by the unit of mA.
It is 33mA if displayed as "0033".

<For DVD>
If the value of the current of the laser is 64mA or less, it is possible to judge simply
with about normal.
The deterioration of the laser diode of picking up is thought when there are 65mA or more
value of the current of the laser.

<For CD>
If the value of the current of the laser is 49mA or less, it is possible to judge simply
with about normal.
The deterioration of the laser diode of picking up is thought when there are 50mA or more
value of the current of the laser.

• Jitter measurement value

FL display(Example)

```
0033   20A2
```
↑
jitter value

The jitter value is displayed by the hex

<Please adjust when corresponding to the following.>

• When you exchange picking up.
• When you replace the spindle motor.
• When the reading accuracy of the signal is low.
(The screen sometimes stops in outer which with the block noise to the screen on the disk)

(2) EEPROM initialization
When the ENTER key is pushed in the test mode; Done the intialize for EEPROM of system CPU and
unit CPU.

FL display

T	E	S	T				D		R	2
		E	E	P	R	O	M			

(3) Inside and outside surroundings tracking OFF
After searches for the DA disk to first TR and each last TR when   " ⏮◄◄ " and the
" ►►⏭ " key are pushed in the test mode, tracking OFF is processed.

(4) Display of number of ROM

When MENU and the TOP MENU key are pushed in the test mode, the number of ROM of the main microcomputer, a sub-microcomputer, the unit microcomputer, and microcode is displayed on the FL display instead of the test display.

Transmission command: C2(ROM VERSION REQUEST)

Data from unit CPU is as follows.

FIX4   BYTE11: Ver subordinate position byte of unit CPU

BYTE12: Ver high-ranking byte of unit CPU (HEX)

BYTE13: Date of microcode(ASCII)

FL display (When you press MENU:five seconds).

Version of unit microcomputer

U	N	I	T	:		0	0	1	9	
M	C	:		1	2	J	A	N	0	0

Microcode

FL display (When you press TOP MENU:five seconds).

Version of the main microcomputer

S	Y	S	:			1	.	0	8	
D	V	D	:			1	.	0	7	

Version of sub-microcomputer

(5) Servo relation examination command

The following processing is done to ten keys in the test mode respectively.

[1] : Start & reproduction of DISC (reproduction from starting position)

[2] : TNO+1 search of CD

[3] : TNO-1 search of CD

[4] : The CD_LD lighting (Turn off with the stop button).

[5] : The DVD_LD lighting (Turn off with the stop button).

[6] : DVDx1.4 jitter measurement mode

[7] : Unused

[8] : The display (The address is done and -1 is done).

[9] : The display (The address is done and +1 is done).

([8] and [9] are the stop button and Back to Top.)

<Cassette mechanism section>

Head angle azimuth screw (foward)

Head angle azimuth screw (reverse)
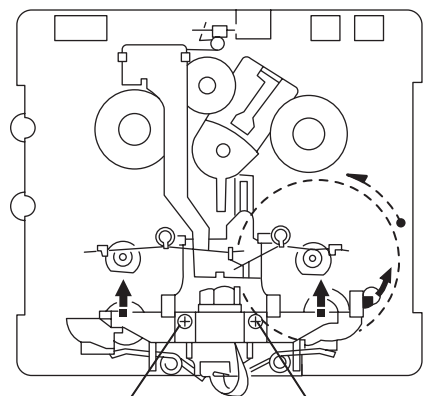
Head angle azimuth screw (foward)

Head angle azimuth screw (reverse)
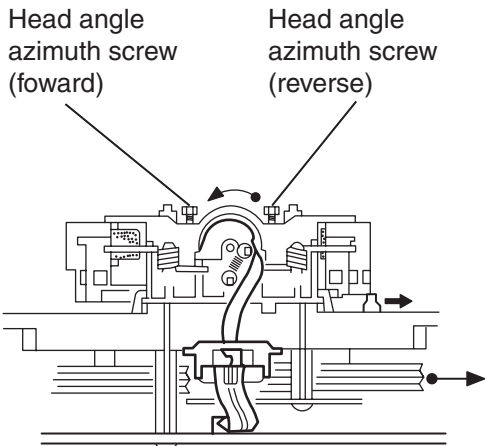
CN31

Recording and play head/Erase head

Mechanism control P.C. board

Motor speed VR37

BIAS adjustment VR31
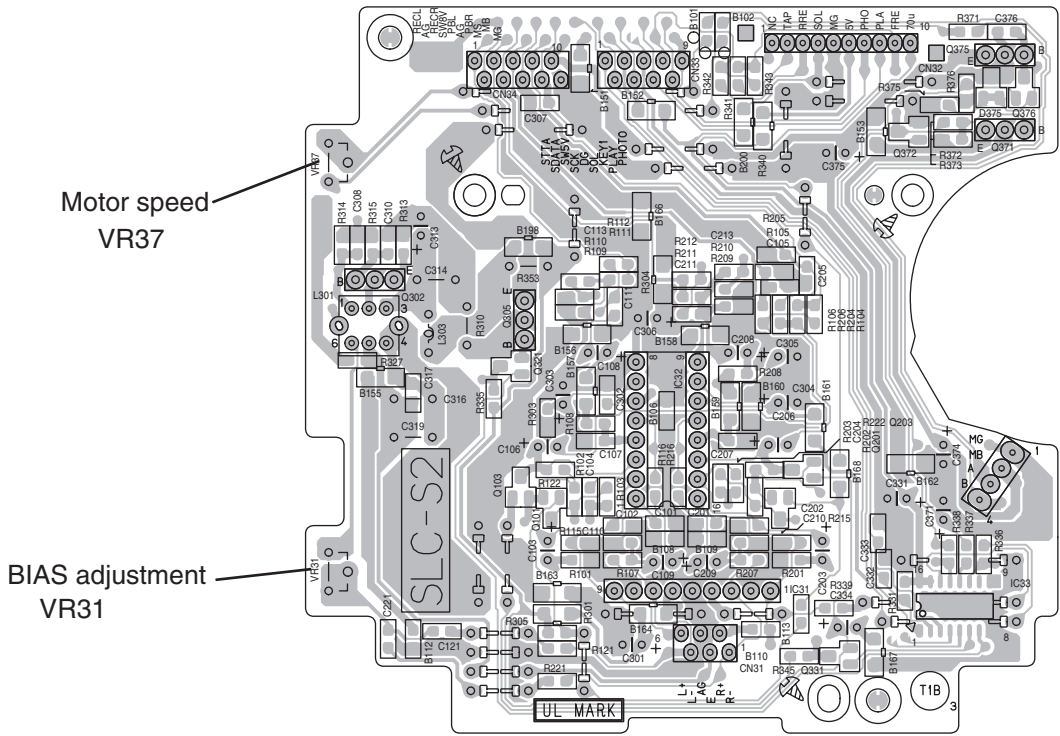
■**Mechanism section**

Item	Confirmation of angle of head	Tape speed confirmation
Mesurement condition	Test tape: VT703L (8kHz) Measurement output terminal: Speaker terminal	Test tape: VT712 (3kHz) Measurement output terminal: Speaker terminal or headphone terminal
Mesurement procedure	1.Test tape VT703L (8kHz) is played. 2.It is adjusted that becomes an output that both are the maximum on a forward side and a reverse side with the screw for the azimuth adjustment. 3.This adjustment is adjusted respectively with the adjustment screw for the forward side and the adjustment screw for a reverse side.	Test tape VT712(3kHz) of the forward is reproduced by finishing rolling , and adjusted for the display of the frequency counter to become 2,940-3,090Hz by VR37.
Standard value	The maximum output	2,940 ~ 3,090Hz
Adjustment position	Only when the head is exchanged, adjusts.	VR37

■**Reference and standard value of confirmation matter**

Item	Forward/reverse tape speed difference	Wow & flutter
Mesurement condition	Test tape: VT712 (3kHz) Measurement output terminal: Speaker terminal or headphone terminal	
Mesurement procedure	Both reverse must forward/reproduce, and the speed difference must be 6.0Hz or less as for finish wrapping of test tape VT712 (3kHz).	Both reverse must forward/reproduce, and each wow & flutter must be 0.25% (WRMS) or less as for begin to wrap of test tape VT712 (3kHz).
Standard value	6.0Hz or less	0.25% or less (WRMS)
Adjustment position	VR31	

■Electric adjustment

Item	Recording BIAS adjustment	Recording reproduction frequency characteristic
Mesurement condition	Forward or reverse Test tape: AC-514 TYPE Ⅱ and 　　　　　AC-225 TYPE Ⅰ Measurement output terminal: Recording and headphone terminal	Standard frequency: 1kHz/10kHz 　　　　　　　　(Srandard: -20dB) Test tape: AC-514 TYPE Ⅱ Measurement input terminal: OSC IN
Mesurement procedure	1.Test tape (AC-514 TYPEⅡ,AC-225 　TYPE Ⅰ)is installed, and makes to 　recording/pose. 2.Connects in the head for the recording 　and to connect 100 with the series and 　to measure the current of the bias, 　connects with VTVM. 3.The pose is released after sets and the 　recording begins. It is adjusted that the 　current of the bias reaches the following 　value by VR31 for L side at this time and 　VR32 for R side. 　4.0μA (TYPE Ⅰ)and4.20μA (TYPEⅡ)	1.Test tape (AC-514 TYPEⅡ)is installed, 　and makes to recording/pose. 2.Records the recording's releasing the 　pose, beginning, and repeating 1kHz 　and 10kHz of a standard frequency from 　the frequency transmitter. 3.VR31 for L side and VR32 for R side are 　adjusted so that the recorded part may 　be reproduced and there is a difference 　between 1kHz and 10kHz in 1dB }2dB, 　and the recording is repeated again.
Standard value	AC-225: 4.20μA AC-514: 4.0μA	Output difference 1kHz/10kHz:-1dB±2dB
Adjustment position	VR31	

■Electric characteristic confirmation

Item	Current of recording bias	Deletion current (standard value)
Mesurement condition	Forward or reverse Test tape: AC-514 TYPE Ⅱ Measurement terminal: 　　　　　BIAS TP on P.C.board	Forward or reverse State of recording Test tape: AC-514 TYPE Ⅱ and 　　　　　　　　　　　　AC-225TYPE Ⅰ Measurement terminal: 　　　　　Erase head's both ends
Mesurement procedure	1. It is confirmed that BIAS1 and 2 are 　switched, and the frequency changes. 2.Test tape (AC-514 TYPE) is installed, 　and recording/makes to the pose. 3.It is confirmed that it is BIAS TP on the 　substrate and the frequency is 100Hz± 　6kHz.	1.Test tape (AC-514 TYPEⅡ)is installed, 　and makes to recording/pose. 2.The pose is released and after sets in 　the state of the recording, 1W is 　confirmed, and connects with the series, 　and the deletion current is confirmed 　from erase head's both ends to the 　erase head.
Standard value	100kHz±6kHz	TYPE Ⅱ：120mA TYPE Ⅰ：75mA
Adjustment position		

Maintenance of MD pickup

1. Cleaning of pickup lens

(1) Prior to changing the pickup, clean the pickup lens.

(2) For cleaning the lens, use the following cotton swab after mearsing it in alcohol.

   Product No. JCB-B4; Manufacturer;Nippon Cotton Swab

2. Confirmation of the service life of laser diode when the service life of the laser diode has been exhausted, the following symptoms will appear.

(1) Recording will become impossible.

(2) The RF output (EFM output and eye pattern amplitude) will become lower.

(3) The drive current required for light emitting of laser diode will be increased.

Confirm the service life according to the following flow chart:
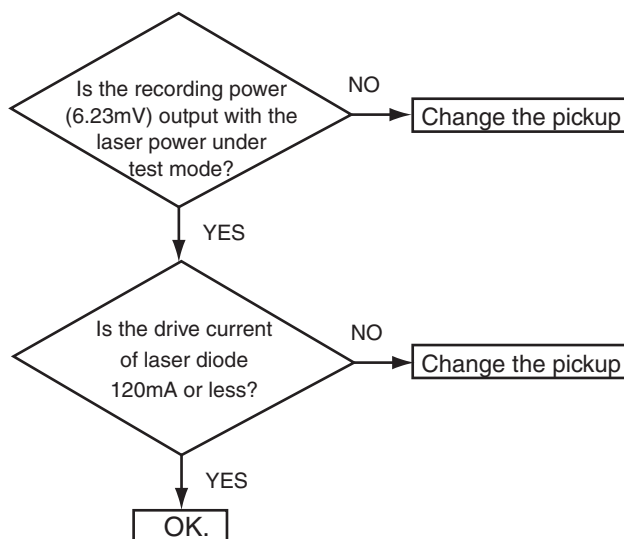
3. Method of measuring the drive current of laser diode

When the voltage measured at both side of R337 of the MD servo P.C. board have become 120mV or over, the service life of the laser diode is judged to have been exhausted.

Procedures of changing the MD pickup
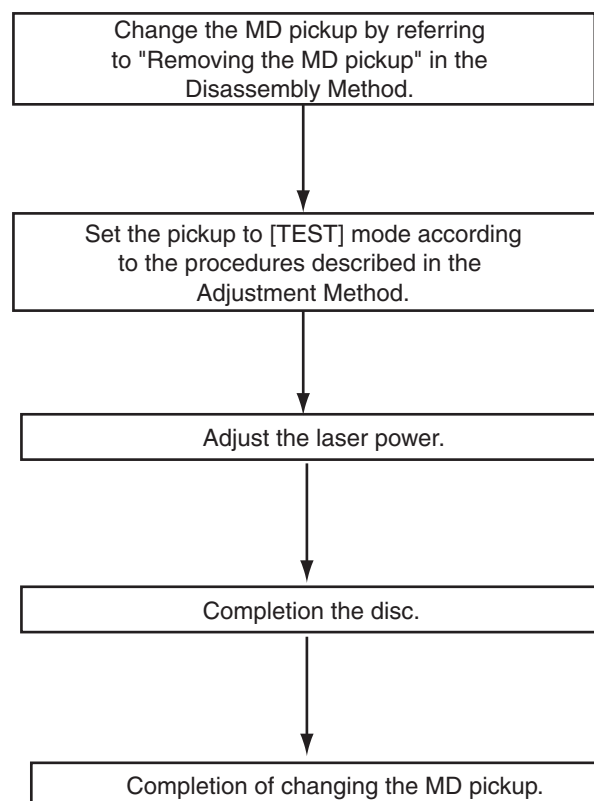
Since this system is designed to perform magnetic recording, the laser power ten times or over of the conventional MD player will be output. Therefore, be sure to perform not only adjustment and operation of this system so carefully as not to directly look at the laser beam or touch on the body.

4. Semi-solid state resistors on the APC P.C. board

The semi-solid state resistor on the APC P.C.board attached to the pickup is used for adjusting the laser power. Since these resistor should be adjusted in pair according to the characteristics of the optical block, be sure not to touch on the resistors.

Since the service life of the laser diode will be exhausted when the laser power is low, it is necessary to change the pickup. Meanwhile, do not pickup. Otherwise, the pickup will be damaged due to over current.

Maintenance of DVD pickup

1. Cleaning of pickup lens

(1) Prior to changing the pickup, clean the pickup lens.

2. Confirmation of the service life of laser diode when the service life of the laser diode has been exhausted, the following symptoms will appear.

(1) The RF output (EFM output and eye pattern amplitude) will become lower.

(2) The drive current required for light emitting of laser diode will be increased.

Confirm the service life according to the following flow chart:

```
                         NO
  ╱─────────────╲  ──────────▶  ┌──────────────────┐
 ╱ Is the RF output╲             │ Change the pickup │
 ╲ 1.25±0.22VP-P?  ╱             └──────────────────┘
  ╲─────────────╱
         │ YES
      ┌──────┐
      │ OK.  │
      └──────┘
```
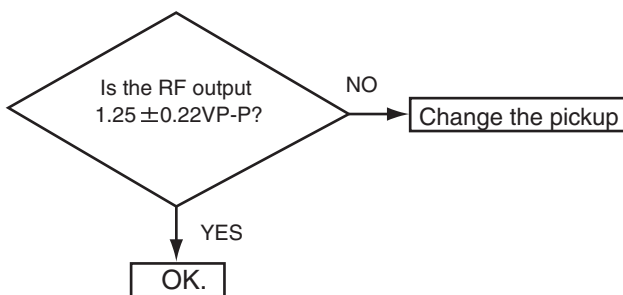
3. Semi-solid state resistors on the APC P.C. board

The semi-solid state resistor on the APC P.C.board attached to the pickup is used for adjusting the laser power. Since these resistor should be adjusted in pair according to the characteristics of the optical block, be sure not to touch on the resistors.

Since the service life of the laser diode will be exhausted when the laser power is low, it is necessary to change the pickup. Meanwhile, do not pickup. Otherwise, the pickup will be damaged due to over current.

Procedures of changing the DVD pickup
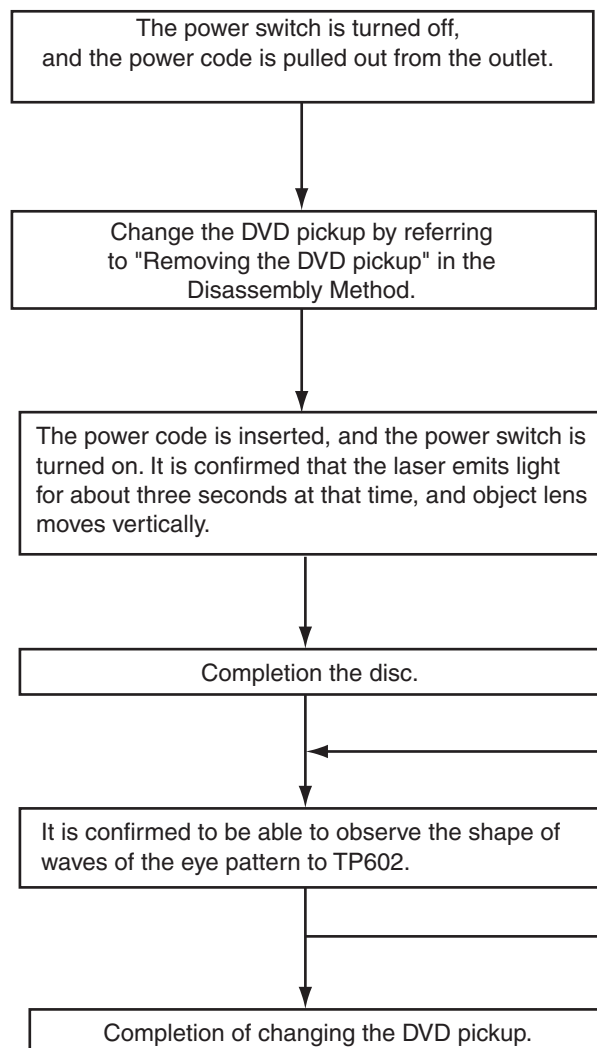
```
┌───────────────────────────────────────┐
│ The power switch is turned off,        │
│ and the power code is pulled out       │
│ from the outlet.                       │
└───────────────────────────────────────┘
                   │
                   ▼
┌───────────────────────────────────────┐
│ Change the DVD pickup by referring     │
│ to "Removing the DVD pickup" in the    │
│ Disassembly Method.                    │
└───────────────────────────────────────┘
                   │
                   ▼
┌───────────────────────────────────────┐
│ The power code is inserted, and the    │
│ power switch is turned on. It is       │
│ confirmed that the laser emits light   │
│ for about three seconds at that time,  │
│ and object lens moves vertically.      │
└───────────────────────────────────────┘
                   │
                   ▼
┌───────────────────────────────────────┐
│ Completion the disc.                   │
└───────────────────────────────────────┘
                   │
                   ▼
┌───────────────────────────────────────┐
│ It is confirmed to be able to observe  │
│ the shape of waves of the eye pattern  │
│ to TP602.                              │
└───────────────────────────────────────┘
                   │
                   ▼
┌───────────────────────────────────────┐
│ Completion of changing the DVD pickup. │
└───────────────────────────────────────┘
```

Therefore, besure to perform not only adjustment and operation of this system so carefully as not to directly look at thelaser beam or touch on the body.

Description of major ICs

■ AK93C65AF-X (IC451) : EEPROM

1.Pin layout

```
        ┌─────────────┐
  PE ──│ 1         8 │── NC
       │             │
 VCC ──│ 2         7 │── GND
       │             │
  CS ──│ 3         6 │── DO
       │             │
  SK ──│ 4         5 │── DI
       └─────────────┘
          8 PIN SOP
```

2.Block diagram

```
┌──────────────────────────────────────────────────────────────────────────┐
│                              ┌──────────┐                          ▷── DO  │
│                              │   DATA   │   ┌──────────┐                    │
│                              │ REGISTER │⟷16│ R/W AMPS │⟷16  ┌──────────┐  │
│        ┌────────────┐  ┌─────┴──────────┘   │   AND    │     │          │  │
│        │INSTRUCTION │  │INSTRUCTION         │AUTO ERASE│     │  EEPROM  │  │
│ DI ────│ REGISTER   │  │  DECODE,           └──────────┘     │          │  │
│        └────────────┘  │ CONTROL            ┌──────────┐     │ 4096bit  │  │
│                        │   AND      ┌─────┐ │ DECODER  │     │ 256 x 16 │  │
│                        │  CLOCK     │ADD. │ │          │     │          │  │
│                        │GENERATION  │BUFF.│ └──────────┘     │          │  │
│ CS ────────────────────│            └─────┘                  │          │  │
│                        │                   ┌──────────┐      │          │  │
│ SK ────────────────────│                   │  VPP SW  │      └──────────┘  │
│                        │                   └──────────┘                    │
│ PE ────────────────────│         ┌──────┐  ┌──────────┐                    │
│                        │         │ VREF │→ │   VPP    │                    │
│                        └─────────│      │  │GENERATOR │                    │
│                                  └──────┘  └──────────┘                    │
└──────────────────────────────────────────────────────────────────────────┘
```
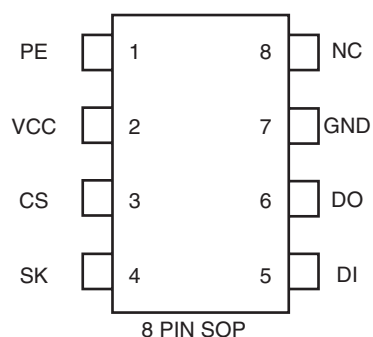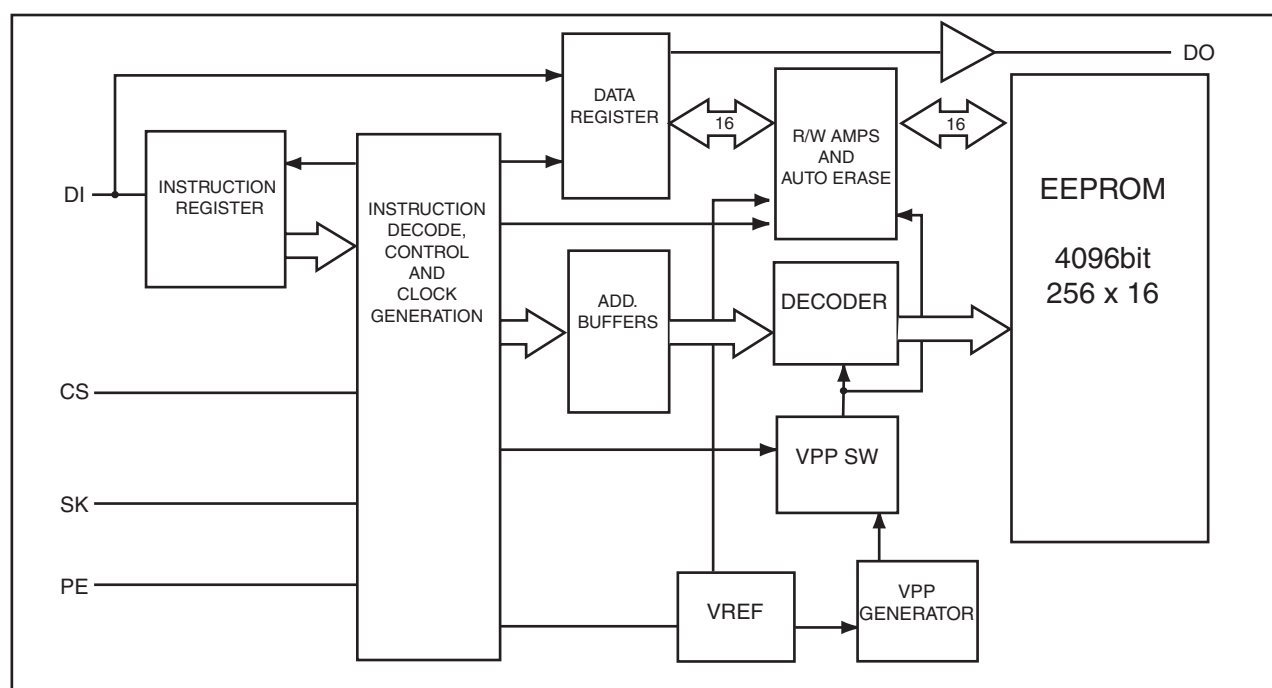
3.Pin function

Pin no.	Symbol	Function
1	PE	Program enable (With built-in pull-up resistor)
2	VCC	Power supply
3	CS	Chip selection
4	SK	Cereal clock input
5	DI	Cereal data input
6	DO	Cereal data output
7	GND	Ground
8	NC	No connection

NOTE : The pull-up resistor of the PE pin is about 2.5M Ω (VCC=5V)

■ 74VHC00MTC-X (IC455,503) : NAND gate

1.Pin layout / Block diagram
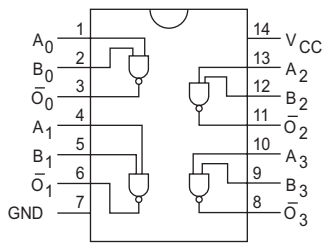
Truth Table

A	B	$\overline{O}$
L	L	H
L	H	H
H	L	H
H	H	L

2.Pin function

Pin Names	function
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

■ 74VHC74MTC-X (IC454) : Dual D-type Flip-Flop with preset and clear

1.Pin layout / Block diagram
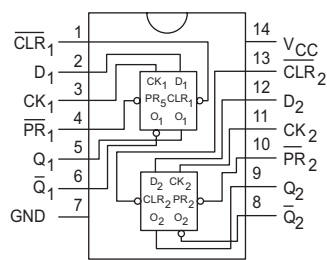
Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H(Note 1)	H(Note 1)	
H	H	L	⤴	L	H	
H	H	H	⤴	H	L	
H	H	X	⤵	Q_n	Q_n	No Change

Note 1: This configurailon is nonstable; that is, it will not persist when pre-
set and clear inputs return to their inactive (HIGH) state.

2.Pin function

Pin Names	function
D_1, D_2	Data Inputs
CK_1, CK_2	Clock Pulse Inputs
$\overline{CLR}_1, \overline{CLR}_2$	Direct Clear Inputs
$\overline{PR}_1, \overline{PR}_2$	Direct Preset Inputs
$Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$	Output

■ BR93LC66F-X (IC590):EEPROM

1.Terminal layout

2.Pin Functions

Symbol	I/O	Function
VCC	-	Power supply
GND	-	Connect to GND
CS	I	Chip select input
SK	I	Serial clock input
DI	I	Start bit,OP-code,address,serial data input
DO	O	Serial data output, Internal state display output of READY/BUSY

■ AK4519VF-X (IC480) : A / D.D / A converter

1.Pin layout
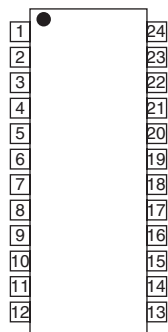
2.Block diagram
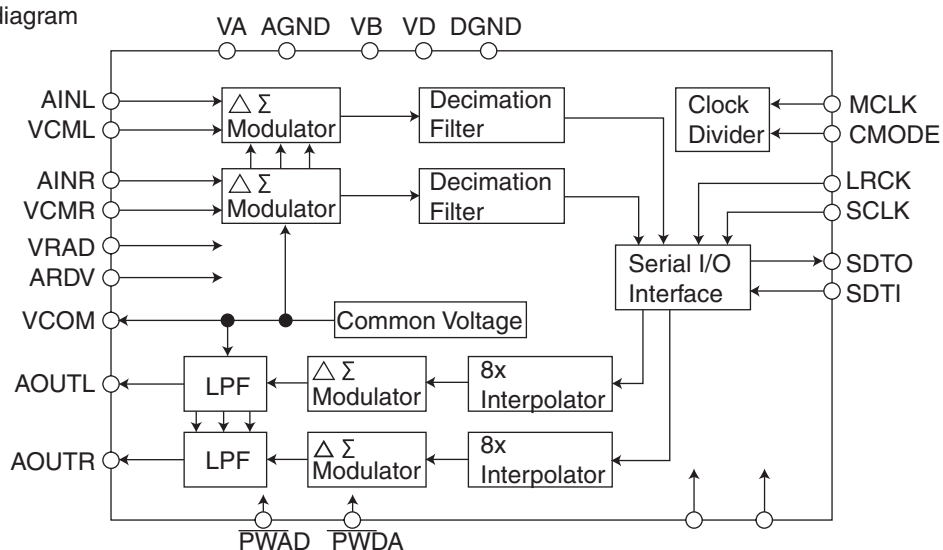
3.Pin Function

Pin NO.	Symbol	I/O	Function
1	VRDA	I	Voltage Reference Input Pin for DAC, VA
2	VRAD	I	Voltage Reference Input Pin for ADC, VA
3	AINR	I	RCH Analog Input Pin
4	VCMR	O	Rch Common Voltage Output Pin, 0.45xVA
5	VCML	O	Lch Common Voltage Output Pin, 0.45xVA
6	AINL	I	Lch Analog Input Pin
7	PWAD	I	ADC Power-Down Mode Pin "L":Power Down
8	PWDA	I	DAC Power-Down Mode Pin "L":Power Down
9	MCLK	I	Master Clock Input Pin
10	LRCK	I	Input/Output Channel Clock Pin
11	SCLK	I	Audio Serial Data Clock Pin
12	SDTO	O	Audio Serial Data Output Pin
13	DGND	-	Digital Ground Pin
14	VD	-	Digital Power Supply Pin
15	SDTI	I	Audio Serial Data Input Pin
16	CMODE	I	Master Clock Select Pin
17	DEM1	I	De-emphasis Frequency Select Pin
18	DEM0	I	De-emphasis Frequency Select Pin
19	AOUTL	O	Lch Analog Output Pin
20	AOUTR	O	Rch Analog Output Pin
21	VCOM	O	Common Voltage Output Pin, 0.45xVA
22	AGND	-	Analog Ground Pin
23	VB	-	Substrate Pin
24	VA	-	Analog Power Supply Pin

■ AN8703FH-V (IC101) : Front-end processor for DVD

1.Pin layout

48~33

49~64   32~17

1~16
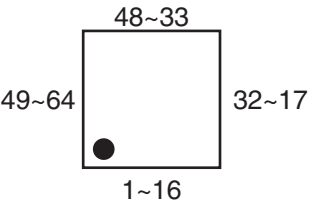
2. Block diagram
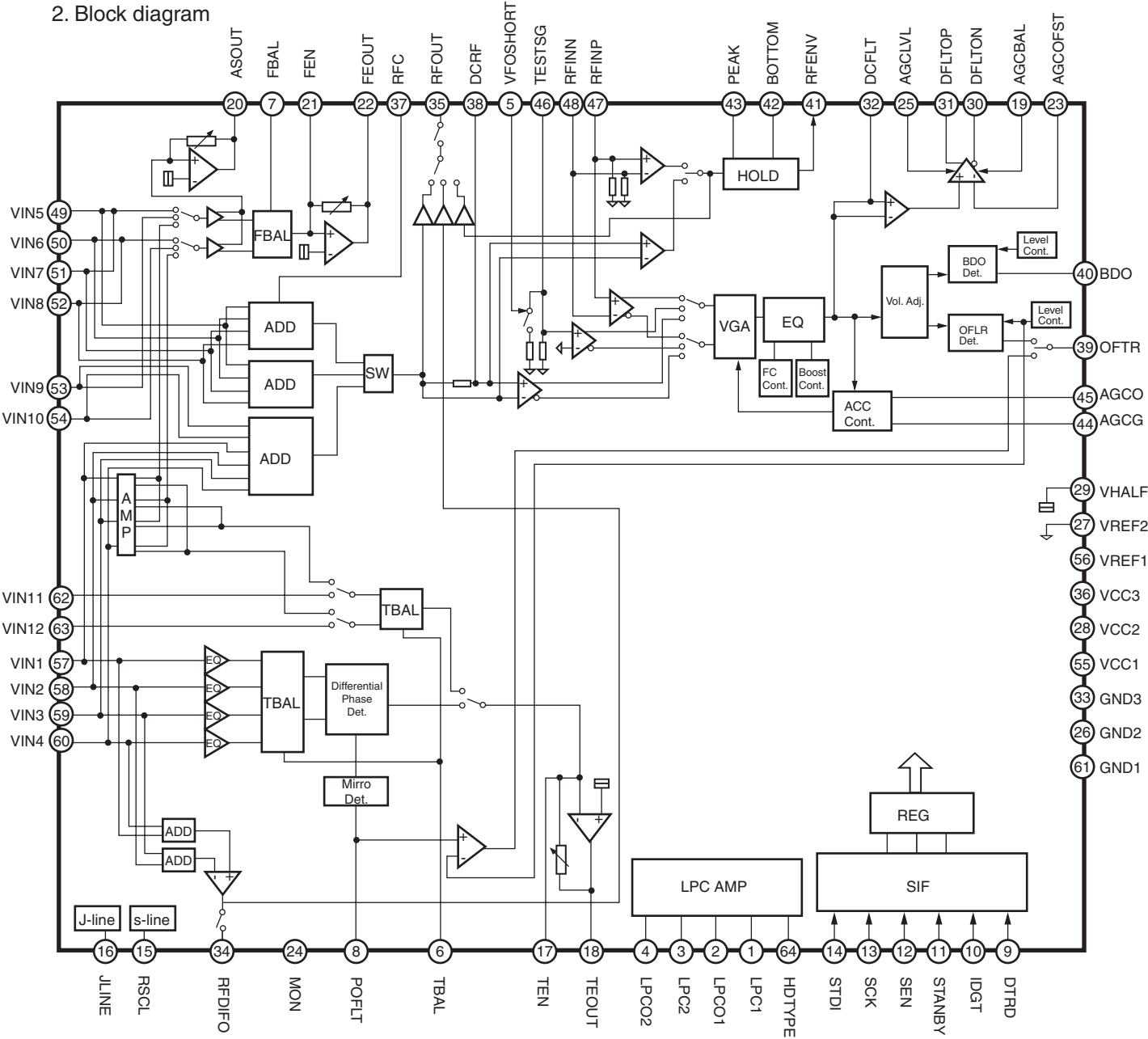
3.Pin function

(1/2)

Pin No.	Symbol	Function
1	LPC1	Laser pin input (DVD head)
2	LPCO1	Laser drive output (DVD head)
3	LPC2	Laser pin input (CD head)
4	LPCO2	Laser drive output (CD head)
5	VFOSHORT	VFOSHORT control
6	TBAL	Tracking balance control
7	FBAL	Focus balance control

3.Pin function   (2/2)

Pin No.	Symbol	Function
8	POFLT	Tracking detection threshold level
9	DTRD	Data slice data read signal input (for RAM)
10	IDGT	Data slice address gate signal input (for RAM)
11	STANBY	Standby mode control
12	SEN	SEN (serial data input)
13	SCK	SCK (serial data input)
14	STDI	STDI (serial data I/o)
15	RSCL	Reference current supply
16	JLINE	J-line current setting
17	TEN	Tracking error amplifier inverted input
18	TEOUT	Tracking error signal output
19	AGCBAL	Offset adjustment for DRC - 1
20	ASOUT	Full addition signal output
21	FEN	Focus error amplifier inverted input
22	FEOUT	Focus error signal output
23	AGCOFST	Offset adjustment for DRC - 2
24	MON	Monitor
25	AGCLVL	Output amplitude adjustment for DRC
26	GND2	Ground 2
27	VREF2	VREF2 voltage output
28	VCC2	Power supply 2 (5V)
29	VHALF	VHALF voltage output
30	DFLTON	Filter amplifier inverted output
31	DFLTOP	Filter amplifier positive output
32	DCFLT	Filter output capacitance connection
33	GND3	Ground3
34	RFDIFO	Radial differential output
35	RFOUT	RF full-addition amplifier output
36	VCC3	Power supply 3 (3.3V)
37	RFC	Filter for RF-group delay correction amplifier
38	DCRF	DC-cut filter for RF full-addition amplifier
39	OFTR	OFTR output
40	BDO	BDO output
41	RFENV	RF envelope output
42	BOTTOM	Bottom envelope detection filter
43	PEAK	Peak envelope detection filter
44	AGCG	AGC amplifier gain control
45	AGCO	AGC amplifier level control
46	TESTSG	TEST signal input
47	RFINP	RF signal positive input
48	RFINN	RF signal inverted input
49	VIN5	Internal four-partition (CD) RF input 1
50	VIN6	Internal four-partition (CD) RF input 2
51	VIN7	Internal four-partition (CD) RF input 3
52	VIN8	Internal four-partition (CD) RF input 4
53	VIN9	External two-partition (DVD) RF input 2
54	VIN10	External two-partition (DVD) RF input 1
55	VCC1	Power supply 1 (5V)
56	VREF1	VREF1 voltage output
57	VIN1	Internal four-partition (DVD) RF input 1
58	VIN2	Internal four-partition (DVD) RF input 2
59	VIN3	Internal four-partition (DVD) RF input 3
60	VIN4	Internal four-partition (DVD) RF input 4
61	GND1	Ground 1
62	VIN11	3-beam sub (CD) input 2
63	VIN12	3-beam sub (CD) input 1
64	HDTYPE	HD type selection

UX-A10DVD

■ BA5983FM-X (IC201) : Driver

1.Pin layout / Block diagram
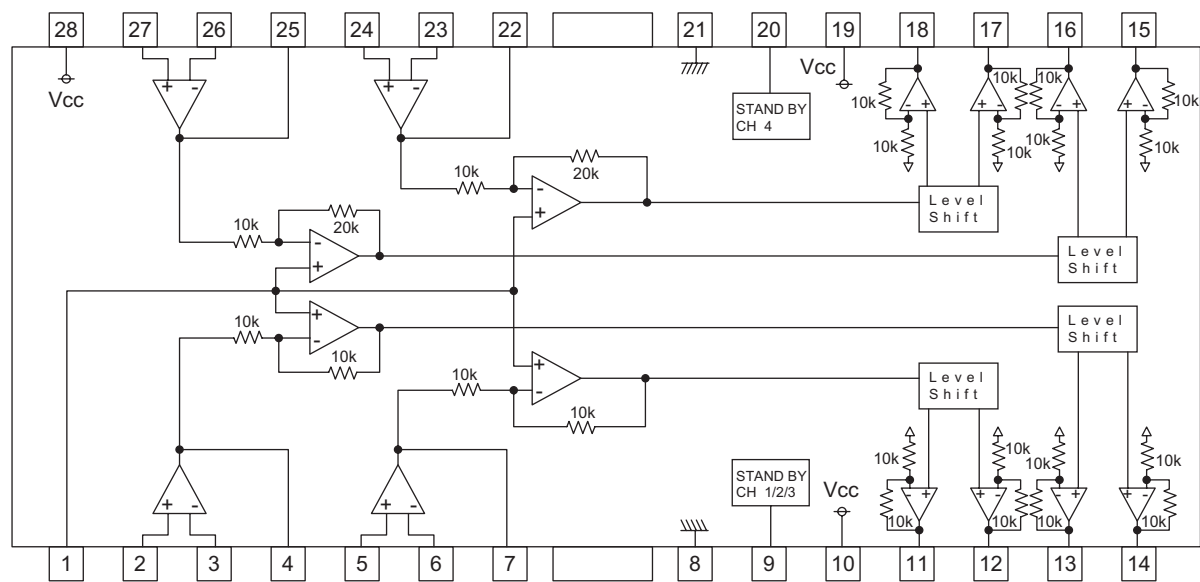
2.Pin function

No.	Symbol	Function	No.	Symbol	Function
1	BIAS IN	Input for Bias-amplifier	15	VO4(+)	Non inverted output of CH4
2	OPIN1(+)	Non inverting input for CH1 OP-AMP	16	VO4(-)	Inverted output of CH4
3	OPIN1(-)	Inverting input for CH1 OP-AMP	17	VO3(+)	Non inverted output of CH3
4	OPOUT1	Output for CH1 OP-AMP	18	VO3(-)	Inverted output of CH3
5	OPIN2(+)	Non inverting input for CH2 OP-AMP	19	PowVcc2	Vcc for CH3/4 power block
6	OPIN2(-)	Inverting input for CH2 OP-AMP	20	STBY2	Input for CH4 stand by control
7	OPOUT2	Output for CH2 OP-AMP	21	GND	Substrate ground
8	GND	Substrate ground	22	OPOUT3	Output for CH3 OP-AMP
9	STBY1	Input for CH1/2/3 stand by control	23	OPIN3(-)	Inverting input for CH3 OP-AMP
10	PowVcc1	Vcc for CH1/2 power block	24	OPIN3(+)	Non inverting input for CH3 OP-AMP
11	VO2(-)	Inverted output of CH2	25	OPOUT4	Output for CH4 OP-AMP
12	VO2(+)	Non inverted output of CH2	26	OPIN4(-)	Inverting input for CH4 OP-AMP
13	VO1(-)	Inverted output of CH1	27	OPIN4(+)	Non inverting input for CH4 OP-AMP
14	VO1(+)	Non inverted output of CH1	28	PreVcc	Vcc for pre block

1-54

■ BA6664FM-X (IC251) : Motor driver

1. Block diagram
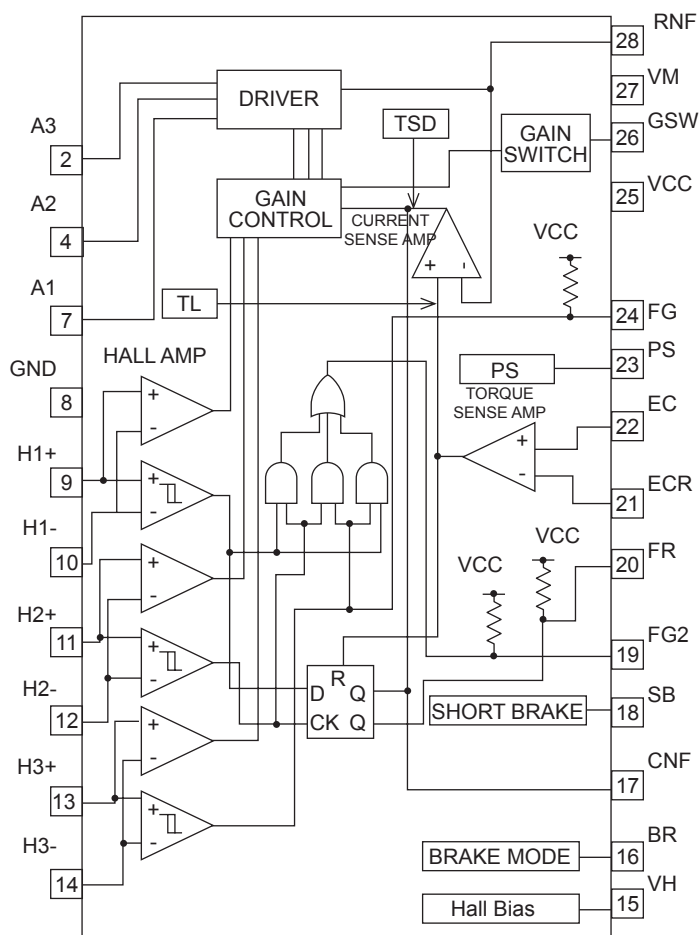
2.Pin function

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	NC	NC	19	FG2	3Phase synthesized FG signal output terminal
2	A3	Output3 for motor	20	FR	Rotation detect signal output terminal
3	NC	NC	21	ECR	Torque control standard voltage input terminal
4	A2	Output2 for motor			
5	NC	NC			
6	NC	NC	22	EC	Torque control voltage input terminal
7	A1	Output1 for motor	23	PS	START/STOP switch
8	GND	GND	24	FG	FG signal output terminal
9	H1+	Positive input for hall input Amp1	25	Vcc	Power supply for signal division
10	H1-	Negative input for hall input Amp1	26	GSW	Gain switch
11	H2+	Positive input for hall input Amp2	27	VM	Power supply for driver division
12	H2-	Negative input for hall input Amp2	28	RNF	Resistance connection pin for output current sense
13	H3+	Positive input for hall input Amp3			
14	H3-	Negative input for hall input Amp3	FIN	FIN	GND
15	VH	Hall bias terminal			
16	BR	Brake Mode terminal			
17	CNF	Capacitor connection pin for phase compensation			
18	SB	Short brake terminal			

■ BD7910FV-X (IC450) : M.HEAD driver

1.Block diagram
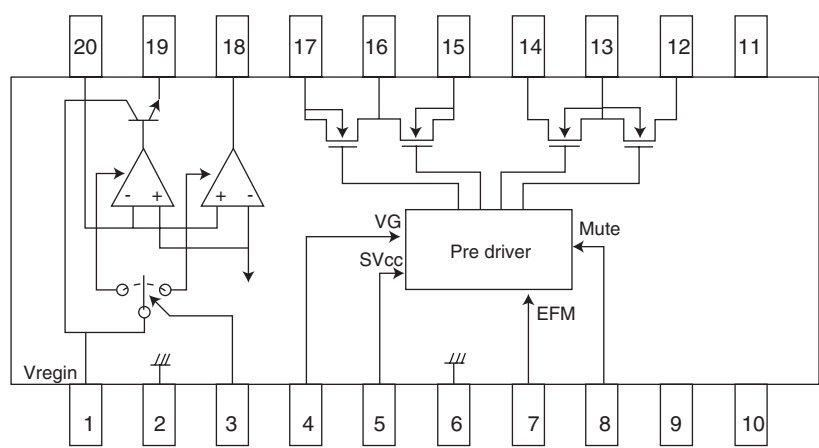
2.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	Vreg IN	I	Regulator input and regulator power supply	11	NC	-	Non connect
				12	VOD2	O	Sync.output (Lower power MOS,drain)
2	Reg GN	-	Regulator GND	13	VSS	-	"H"bridge GND (Lower power MOS,source)
3	NC	-	Non connect	14	VOD1	O	Sync.output (Lower power MOS,drain)
4	VG	I	Voltage input for power MOS drive	15	VOS1	O	Source output (Upper power MOS,source)
5	SVCC	O	EFM high level output voltage	16	VDD	-	"H" bridge power supply terminal (Upper power MOS,source)
6	PDGND	-	Pre-driver GND				
7	EFM	I	EFM signal input	17	VOS2	O	Source output (Upper power MOS,source)
8	MUTE	I	Mute control (Low active)	18	Reg DRV	O	External PNP drive output for regulator
9	NC	O	Non conncet	19	Reg OUT	O	Reglator output (Emitter follower output)
10	NC	O	Non connect	20	Reg NF	-	Regulator feedbaack terminal

■ CS5960AT-X (IC571) : MPEG/Audio clock generator with VCXO

1.Pin layout

```
1 XIN  □        □ 8 XOUT
2 VDD  □        □ 7 27 MHz
3 VCXO □        □ 6 13.5 MHz
4 VSS  □        □ 5 16.93421053 MHz
```
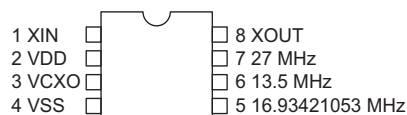
2.Block diagram
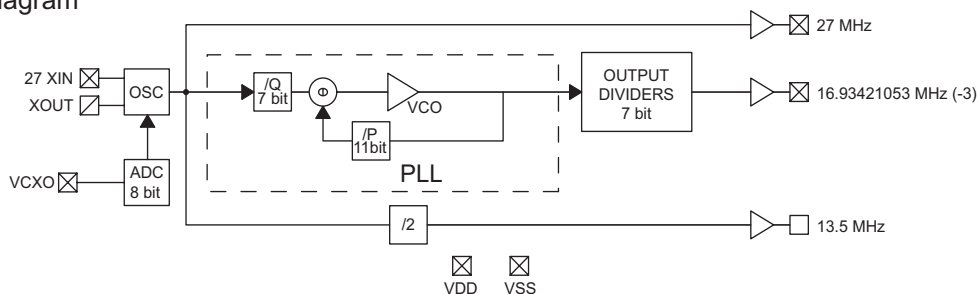
3.Pin function

No.	Symbol	Function
1	XIN	Reference Crystal Input
2	VDD	Voltage Supply
3	VCXO	Input Analog Control for VCXO
4	VSS	Ground
5	16.93421053 MHz	16.93421053-MHz clock output
6	13.5 MHz	13.5-MHz clock output
7	27 MHz	27-MHz clock output
8	XOUT	Reference Crystal output

■ GM71VS17400CLT5 (IC390) : DRAM

1.Pin layout
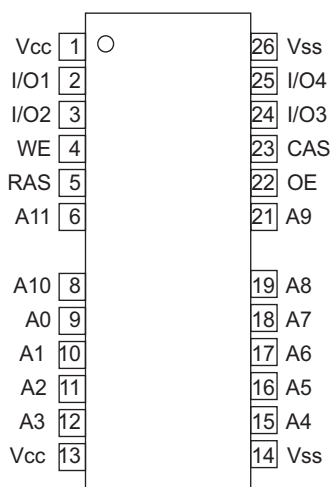
3.Pin function

Pin No.	Symbol	Function
1	Vcc	Power(+3.3V)
2	I/O1	Data-Input/Output
3	I/O2	Data-Input/Output
4	WE	Read/Write Enable
5	RAS	Row Address Strobe
6	A11	Address Input
7	-	No Connection
8	A10	Address Input
9～12	A0～A3	Address Input
13	Vcc	Power(+3.3V)
14	Vss	Ground
15～19	A4～A8	Address Input
20	-	No Connection
21	A9	Address Input
22	OE	Output Enable
23	CAS	Column Address Strobe
24	I/O3	Data-Input/Output
25	I/O4	Data-Input/Output
26	Vss	Ground

■ CXA2523AR (IC310) : MD servo

1.Block diagram
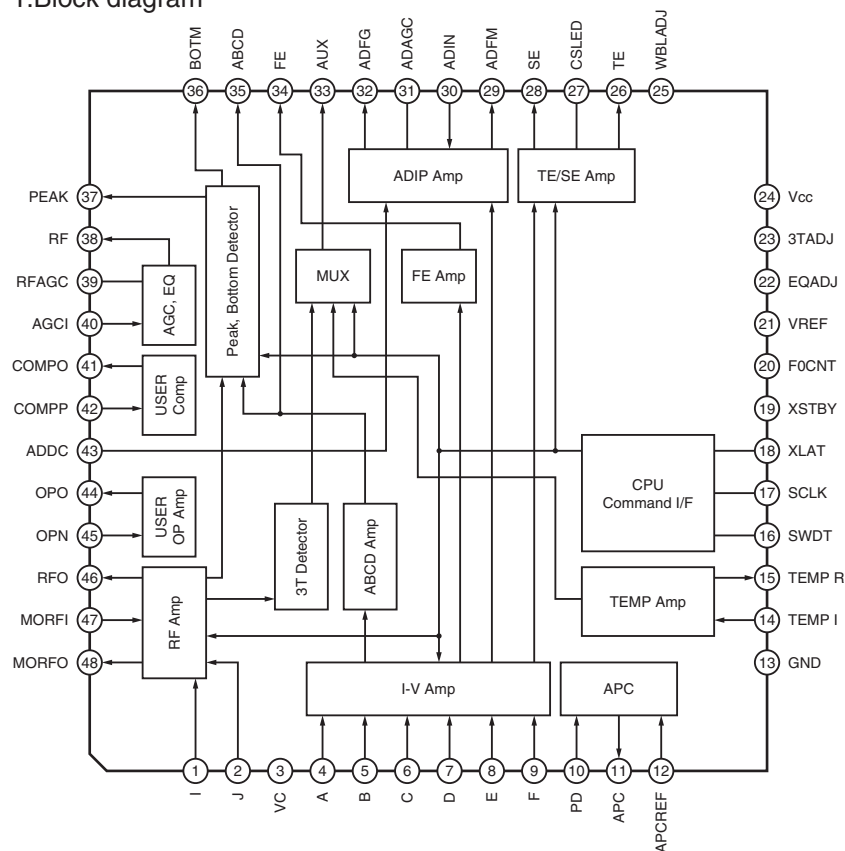
2.Pin function   1/2

Pin No.	Symbol	I/O	Function
1	I	I	I-V converted RF signal I input.
2	J	I	I-V converted RF signal J input.
3	VC	O	Vcc/2 voltage output.
4	A	I	A current input for main beam servo signal.
5	B	I	B current input for main beam servo signal.
6	C	I	C current input for main beam servo signal.
7	D	I	D current input for main beam servo signal.
8	E	I	E current input for side beam servo signal.
9	F	I	F current input for side beam servo signal.
10	PD	I	Reflection light quantity monitor signal input.
11	APC	O	Laser APC output.
12	APCREF	I	Reference voltage input for the laser power intensity setting.
13	GND	-	Connect to GND.
14	TEMPI	I	Connects the temperature sensor.
15	TEMP R	I	Connects the temperature sensor. outputs the reference voltage.
16	SWDT	I	Data input for microcomputer serial interface.
17	SCLK	I	Shift clock input for microcomputer serial interface.
18	XLAT	I	Latch signal input for microcomputer serial interface.Latched when low.
19	XSTBY	I	Standby setting pin. Normal operation when high Standby when low.
20	F0CNT	I	Internal current source setting pin.

2.Pin function   2/2

Pin No.	Symbol	I/O	Function
21	VREF	O	Reference voltage output.
22	EQADJ	I/O	Equalizer center frequency setting pin.
23	3TADJ	I/O	BPF3T center frequency setting pin.
24	Vcc	-	Power supply.
25	WBLADJ	I/O	BPF22 center frequency setting pin.
26	TE	O	Tracking error signal output.
27	CSLED	-	Connects the sled error signal LPF capacitor.
28	SE	O	Sled error signal output.
29	ADFM	O	ADIP FM signal output.
30	ADIN	I	ADIP signal comparator input.
31	ADAGC	-	Connects the ADIPAGC capacitor.
32	ADFG	O	ADIP2 binary value signal output.
33	AUX	O	13 output / temperature signal output. Switched with serial commands.
34	FE	O	Focus error signal output.
35	ABCD	O	Reflection light quantity signal output for the main beam servo detector.
36	BOTM	O	RF/ABCD bottom hold signal output.
37	PEAK	O	Peak hold signal output for the RF/ABCD signals.
38	RF	O	RF equalizer output.
39	RFAGC	-	Connects the RFAGC capacitor.
40	AGCI	I	RFAGC input.
41	COMPO	O	User comparator output.
42	COMPP	I	User comparator non-inverted input.
43	ADDC	I/O	Connects the capacitor for ADIP amplifier feedback circuit.
44	OPO	O	User operational amplifier output.
45	OPN	I	User operational amplifier inverted input.
46	RFO	O	RF amplifier output. Eye pattern checkpoint.
47	MORFI	I	Input of the groove RF signal with AC coupling.
48	MORFO	O	Groove RF signal output.

UX-A10DVD

■ CXD2662R (IC350) : MD DSP

1.Pin layout

```
        75    ~    51
   76              50
   ~               ~
   100             26

   ○   1    ~    25
```

2.Block diagram

1-60
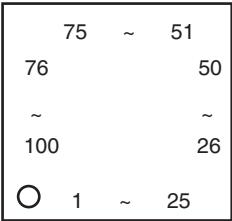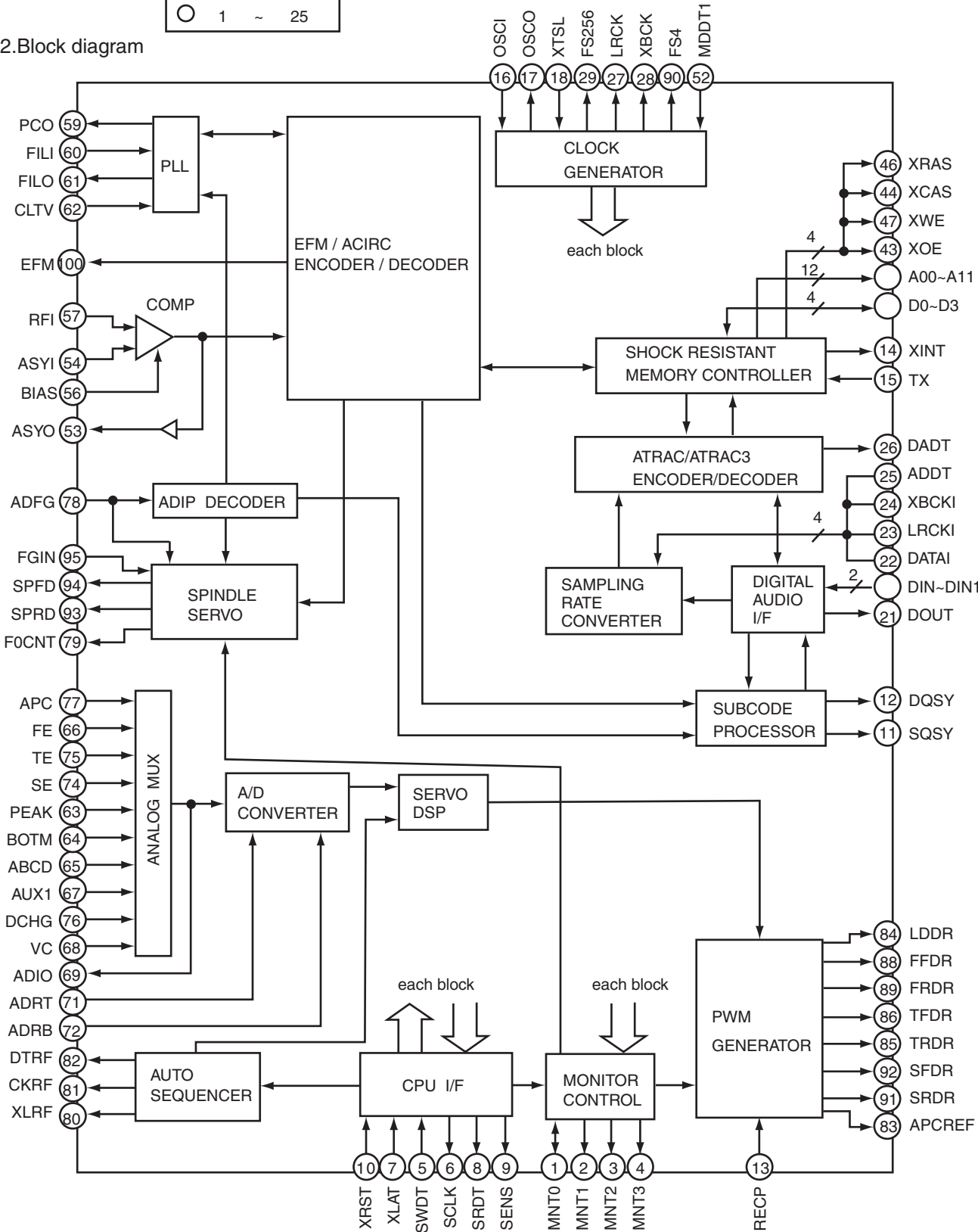
3.Pin function   1/3

Pin No.	Symbol	I/O	Function
1	MNT0	I/O	Monitor output.
2	MNT1	O	Monitor output.
3	MNT2	O	Monitor output.
4	MNT3	O	Monitor output.
5	SWDT	I	Data input for microcomputer serial interface.
6	SCLK	I	Shift clook input for microcomputer serial interface.
7	XLAT	I	Latch input for microcomputer serial interface.Latched at the falling edge.
8	SRDT	O	Data output for microcomputer serial interface.
9	SENS	O	Outputs the internal status corresponding to the microcomputer serial interface address.
10	XRST	I	Reset input. Low : reset
11	SQSY	O	Disc subcode Q sync / ADIP sync output.
12	DQSY	O	Subcode Q sync output in U-bit CD or MD format when the Digital In source is CD or MD.
13	RECP	I	Laser power switching input. High : recording power ; low ; playback power
14	XINT	O	Interruption request output. Low when the interruption status occurs.
15	TX	I	Enable signal input for recoding data output. High : enabled
16	OSCI	I	Crystal oscillation circuit input.
17	OSCO	O	Crystal oscillation circuit output. (inverted output of the OSCI pin)
18	XTSL	I	OSCI input frequency switching. XTSL1(command) = low and XTSL = high : 512Fs (22.5792MHz) XTSL1(command) = low and XTSL = low : 1024Fs (45.1584MHz) XTSL1(command) = high : 2048Fs (90.3168MHz)
19	DIN0	I	Digital audio interface signal input 1.
20	DIN1	I	Digital audio interface signal input 2.
21	DOUT	O	Digital audio interface signal output.
22	DATAI	I	Test pin. Connect to GND.
23	LRCKI	I	Test pin. Connect to GND.
24	XBCKI	I	Test pin. Connect to GND.
25	ADDT	I	Data input from A / D converter.
26	DADT	O	REC monitor output / decoded audio data output.
27	LRCK	O	LA clock (44.1kHz) output to the external audio block.
28	XBCK	O	Bit clock (2.8224kHz) output to the external audio block.
29	FS256	O	256Fs output.
30	DVDD	-	Digital power supply.
31	A03	O	External DRAM address output.
32	A02	O	External DRAM address output.
33	A01	O	External DRAM address output.
34	A00	O	External DRAM address output.
35	A10	O	External DRAM address output.
36	A04	O	External DRAM address output.
37	A05	O	External DRAM address output.
38	A06	O	External DRAM address output.
39	A07	O	External DRAM address output.
40	A08	O	External DRAM address output.
41	A11	O	External DRAM address output.
42	DVSS	-	Digital ground.
43	XOE	O	External DRAM output enable.

3.Pin function   2/3

Pin No.	Symbol	I/O	Function
44	XCAS	O	External DRAM CAS output.
45	A09	O	External DRAM address output.
46	XRAS	O	External DRAM RAS output.
47	XWE	O	External DRAM write enable.
48	D1	I/O	External DRAM data bus.
49	D0	I/O	External DRAM data bus.
50	D2	I/O	External DRAM data bus.
51	D3	I/O	External DRAM data bus.
52	MDDTI	I	MD-DATA mode 1 switching input. (Low : normal mode ; high : MD-DATA mode 1)
53	ASYO	O	Playback EFM full-swing input. (Low : vss ; high : Vdd)
54	ASYI	I	Playback EFM comparator slice voltage input.
55	AVDD	-	Analog power supply.
56	BIAS	I	Playback EFM comparator bias current input.
57	RFI	I	Playback EFM RE signal input.
58	AVSS	-	Analog ground.
59	PCO	O	Phase comparison output for master PLL of playback digital PLL and recording EFM PLL.
60	FILI	I	Filter input for master PLL of playback digital PLL and recording EFM PLL.
61	FILO	O	Filter output for master PLL of playback digital PLL and recording EFM PLL.
62	CLTV	I	Internal VCO control voltage input for master PLL of playback digital EFM PLL and recording EFM PLL.
63	PEAK	I	Peak hold signal input for quantity of light.
64	BOTM	I	Bottom hold signal input for quantity of light.
65	ABCD	I	Signal input for quantity of light.
66	FE	I	Focus error signal input.
67	AUXI	I	Auxillary input 1.
68	VC	I	Center voltage input.
69	ADIO	I	Monitor output for A / D converter input signal.
70	AVDD	-	Analog power supply.
71	ADRT	I	Voltage input for the upper limit of the A / D converter operating range.
72	ADRB	I	Voltage input for the lower limit of the A / D converter operating range.
73	AVSS	-	Analog ground.
74	SE	I	Sled error signal input.
75	TE	I	Tracking error signal input.
76	DCHG	I	Connect to he low-inpedance power supply.
77	APC	I	Error signal input for laser digital APC.
78	ADFG	I	ADIP binary FM signal (22.05 ± 1kHz) input.
79	F0CNT	O	CXA2523 current source setting output.
80	XLRF	O	CXA2523 control latch output. Latched at the falling edge.
81	CKRF	O	CXA2523 control shift clock output.
82	DTRF	O	CXA2523 control data output.
83	APCREF	O	Reference PWM output for laser APC.
84	LDDR	O	PWM output for laser digital APC.
85	TRDR	O	Tracking servo drive PWM output. ($-$)
86	TFDR	O	Tracking servo drive PWM output. (+)
87	DVDD	-	Digital power supply.
88	FFDR	O	Focus servo drive PWM output. (+)
89	FRDR	O	Focus servo drive PWM output. ($-$)
90	FS4	O	4Fs output. (176.4kHz)

3.Pin function   3/3

Pin No.	Symbol	I/O	Function
91	SRDR	O	Sled servo drive PWM output. (−)
92	SFDR	O	Sled servo drive PWM output. (+)
93	SPRD	O	Spindle servo drive output. (PWM (−) or polarity)
94	SPFD	O	Spindle servo drive output. (PWM (+) or PWM absolute value)
95	FGIN	I	Spindle CAV servo FG input.
96	TEST1	I	Test pin. Connect to GND.
97	TEST2	I	Test pin. Connect to GND.
98	TEST3	I	Test pin. Connect to GND.
99	DVSS	-	Digital ground.
100	EFMO	O	Low when playback ; EFM (encoded data) output when recording.

■ CD4094BC (IC33) : Buffer

1.Pin layout

```
STROBE   1      16   VDD
  DATA   2      15   OUTPUT/ENABLE
 CLOCK   3      14   Q5
    Q1   4      13   Q6
    Q2   5      12   Q7
    Q3   6      11   Q8
    Q4   7      10   Q's
   VSS   8       9   Qs
```

2.Truth Table

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Qs (Note 1)	Q'$_\Sigma$
⤒	0	X	X	Hi-Z	Hi-Z	Q7	No Change
⤓	0	X	X	Hi-Z	Hi-Z	No Change	Q7
⤒	1	0	X	No Change	No Change	Q7	No Change
⤒	1	1	0	0	Q_{N-1}	Q7	No Change
⤒	1	1	1	1	Q_{N-1}	Q7	No Change
⤓	1	1	1	No Change	No Change	No Change	Q7

X=Don't Care
⤓ =HIGH-to-LOW
⤒ =LOW-to-HIGH
Note 1: At the positive clock edge,information in the 7th shift register stage is transferred to Q8 and Qs

3.Block Diagram
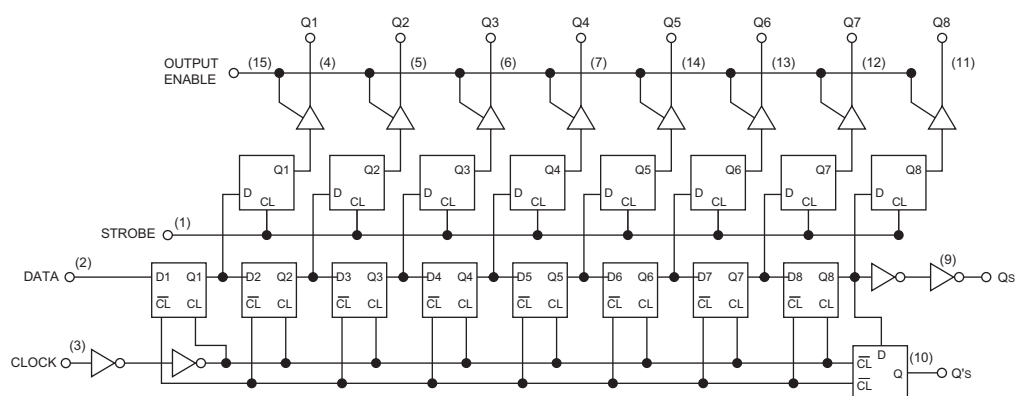
■ GP1FA550RZ (IC391) : Fiber-optic receiver unit

1.Pin layout
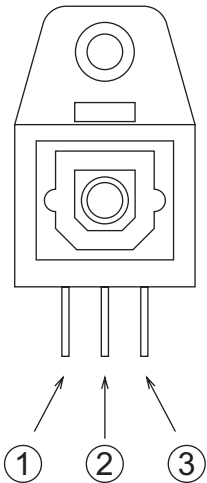
2.Pin function / Block diagram

① VCC

③ Vout

② GND

comp & output circuit

※ 1 OPIC light detector

① ② ③
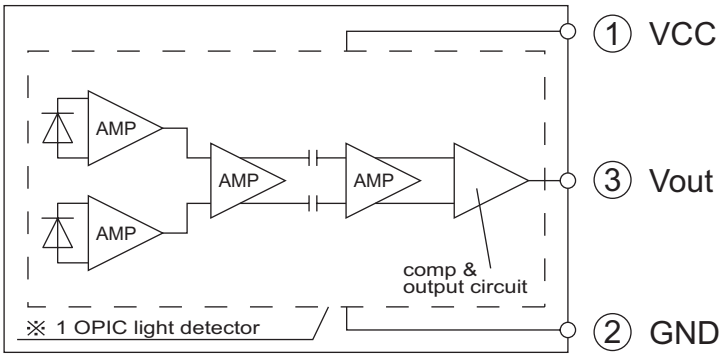
■ GP1FA550TZ (IC392) : Fiber-optic transmitter unit

1.Pin layout
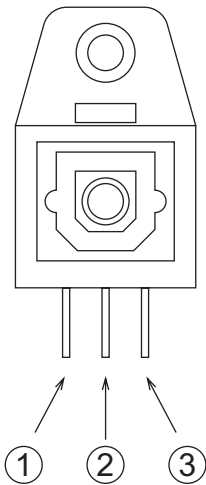
2.Pin function

① Vin

② Vcc

③ GND

① ② ③

■ GP1UM261XK (IC861) : IR detect unit

1. Pin layout

Vout GND
     Vcc

2. Block diagram

Amp Limiter B.P.F. Integrator

Demodulator Comparator

GND Vdd Vout
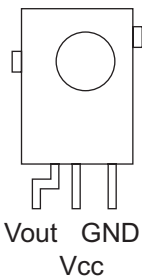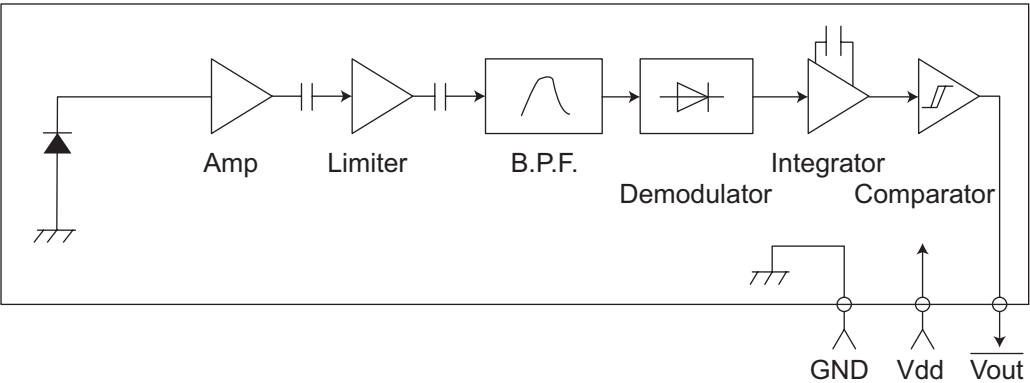
■ HA12238F (IC32) : Recording / Reproduction Equalizer

1.Block diagram
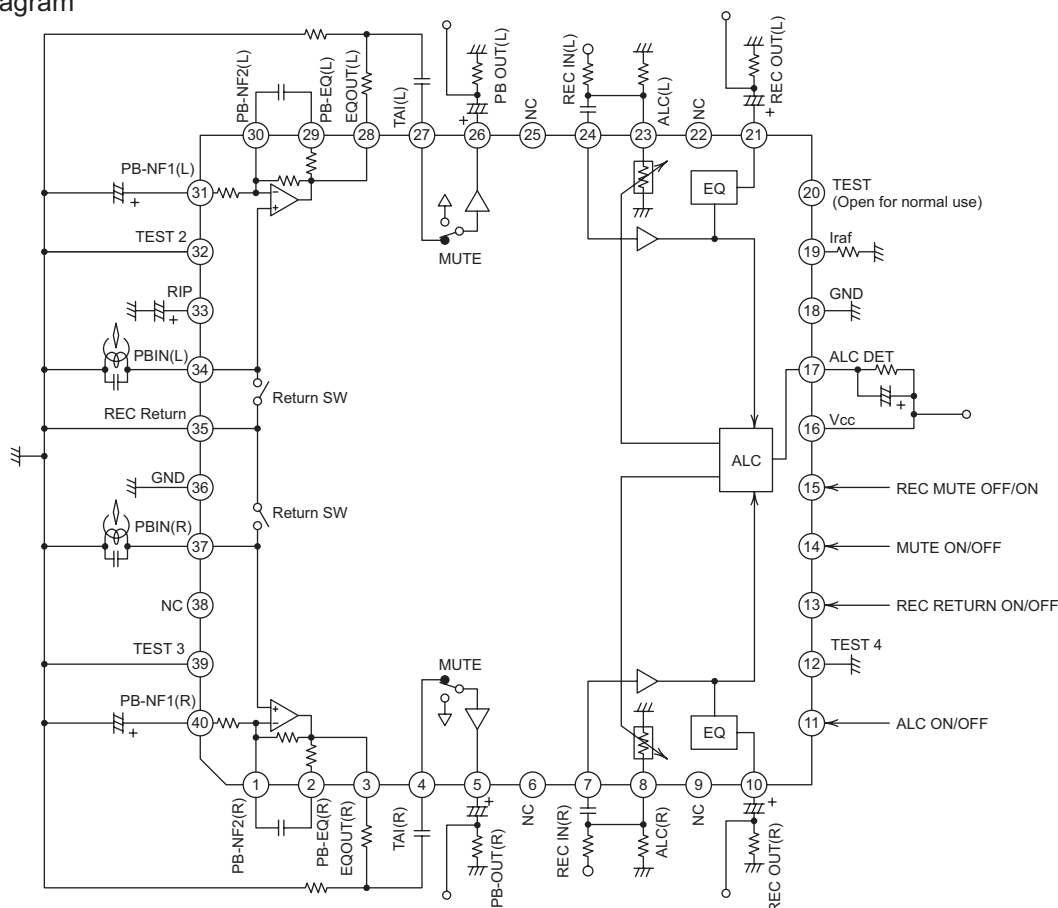
2.Pin function

Pin No.	Symbol	I/O	function
1	PB-NF2(R)	-	Reproduction equalizer feedback terminal
2	PB-EQ(R)	O	NAB output terminal
3	EQ OUT(R)	O	EQ output terminal
4	TAI(R)	I	Tape input terminal
5	PB OUT(R)	O	Reproduction output terminal
6	NC	-	Unused
7	REC IN(R)	I	Input terminal
8	ALC(R)	I	ALC(R) Input terminal
9	NC	-	Unused
10	REC OUT(R)	O	REC output terminal
11	ALC ON/OFF	I	Mode control input terminal
12	TEST4	-	Test terminal
13	REC Return ON/OFF	I	Mode control input terminal
14	MUTE ON/OFF	I	Mode control input terminal
15	REC MUTE OFF/ON	I	Mode control input terminal
16	Vcc	-	Vcc terminal
17	ALC DET	-	ALC detection terminal
18	GND	-	Grand terminal
19	IREF	I	Equalizer standard current input terminal
20	Test mode	-	Test mode terminal

Pin No.	Symbol	I/O	function
21	REC OUT(L)	O	REC output terminal
22	NC	-	Unused
23	ALC(L)	I	ALC(L)input terminal
24	REC IN(L)	I	REC-EQ input terminal
25	NC	-	Unused
26	PB OUT(L)	O	Reproduction output terminal
27	TAI(L)	I	Tape input terminal
28	EQ OUT(L)	O	EQ output terminal
29	PB-EQ(L)	O	NAB output terminal
30	PB-NF2(L)	-	Reproduction equalizer feedback terminal
31	PB-NF1(L)	-	Reproduction equalizer feedback terminal
32	TEST2	-	Test terminal
33	RIP	-	Ripple filter terminal
34	PBIN(L)	I	Reproduction input terminal
35	REC-RETURN	-	REC return terminal
36	GND	-	Grand terminal
37	PBIN(R)	I	Reproduction input terminal
38	NC	-	Unused
39	TEST3	-	Test terminal
40	PB-NF1(R)	-	Reproduction equalizer feedback terminal

UX-A10DVD

■ K4S641632F-TC75 (IC504) : SDRAM

1.Pin layout

Top pins (left to right, 54 to 28):

Pin	Name
54	VSS
53	DQ15
52	VSSQ
51	DQ14
50	DQ13
49	VDDQ
48	DQ12
47	DQ11
46	VSSQ
45	DQ10
44	DQ9
43	VDDQ
42	DQ8
41	VSS
40	N.C/RFU
39	UDQM
38	CLK
37	CKE
36	N.C
35	A11
34	A9
33	A8
32	A7
31	A6
30	A5
29	A4
28	VSS

Bottom pins (left to right, 1 to 27):

Pin	Name
1	VDD
2	DQ0
3	VDDQ
4	DQ1
5	DQ2
6	VSSQ
7	DQ3
8	DQ4
9	VDDQ
10	DQ5
11	DQ6
12	VSSQ
13	DQ7
14	VDD
15	LDQM
16	WE
17	CAS
18	RAS
19	CS
20	BA0
21	BA1
22	A10/AP
23	A0
24	A1
25	A2
26	A3
27	VDD

2.Block diagram

*Samsung Electronics reserves the right to change products or specification without notice.

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3.Pin function

K4S641632F-TC75

Pin No.	Symbol	Function
1	VDD	Power and ground for the input buffers and the core logic.
2	DQ0	Data inputs/outputs are muitiplexed on the same plns.
3	VDDQ	Isolated power supply and ground for the output buffers to provide improved noise Immunity.
4,5	DQ1,DQ2	Data inputs/outputs are muitiplexed on the same plns.
6	VSSQ	Isolated power supply and ground for the output buffers to provide improved noise Immunity.
7,8	DQ3,DQ4	Data inputs/outputs are muitiplexed on the same plns.
9	VDDQ	Isolated power supply and ground for the output buffers to provide improved noise Immunity.
10,11	DQ5,DQ6	Data inputs/outputs are muitiplexed on the same plns.
12	VSSQ	Isolated power supply and ground for the output buffers to provide improved noise Immunity.
13	DQ7	Data inputs/outputs are muitiplexed on the same plns.
14	VDD	Power and ground for the input buffers and the core logic.
15	LDQM	Makes data output Hi-Z, tsHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
16	WE	Enables wnite operation and row precharge. Latches data in starting from CAS,WE active.
17	CAS	Latches column addresses on the positlve going edge of the CLK with CAS low. Enables column access.
18	RAS	Latches row addresses on the positlve going edge of the CLK with RAS low. Enables row access & precharge.
19	CS	Disables or enables device oparation by masking or enabling all inputs except CLK,CKE and L(U)DQM
20,21	BA0,BA1	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
22~26	A10/AP, A0~A3	Row/column addresses are multiplexed on the same plns. Row address : RA0~RA11, Column address : CA0~CA7
27,28	VDD,VSS	Power and ground for the input buffers and the core logic.
29~35	A4~A9, A11	Row/column addresses are multiplexed on the same plns. Row address : RA0~RA11, Column address : CA0~CA7
36	N.C	This pin is recommended to be left No Connection on the device.
37	CKE	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Dlsable input buffers for power down in standby.
38	CLK	Active on the positlve going edge to sample all inputs.
39	UDQM	Makes data output Hi-Z, tsHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
40	N.C/RFU	This pin is recommended to be left No Connection on the device.
41	VSS	Power and ground for the input buffers and the core logic.
42	DQ8	Data inputs/outputs are muitiplexed on the same plns.
43	VDDQ	Isolated power supply and ground for the output buffers to provide improved noise Immunity.
44,45	DQ9,DQ10	Data inputs/outputs are muitiplexed on the same plns.
46	VSSQ	Isolated power supply and ground for the output buffers to provide improved noise Immunity.
47,48	DQ11,DQ12	Data inputs/outputs are muitiplexed on the same plns.
49	VDDQ	Isolated power supply and ground for the output buffers to provide improved noise Immunity.
50,51	DQ13,DQ14	Data inputs/outputs are muitiplexed on the same plns.
52	VSSQ	Isolated power supply and ground for the output buffers to provide improved noise Immunity.
53	DQ15	Data inputs/outputs are muitiplexed on the same plns.
54	VSS	Power and ground for the input buffers and the core logic.

UX-A10DVD

■ L4909 (IC212) : Regulator

1. Pin layout
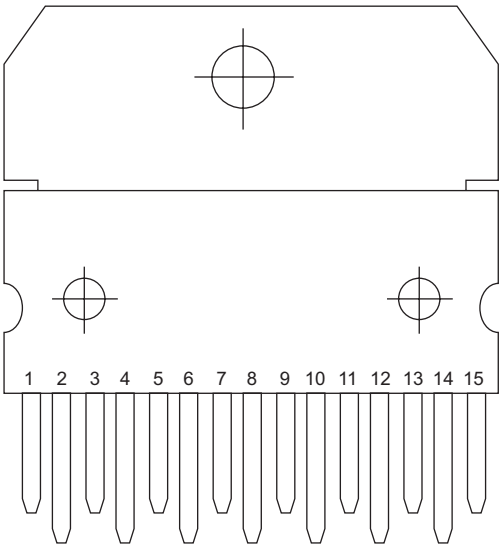
2. Block diagram
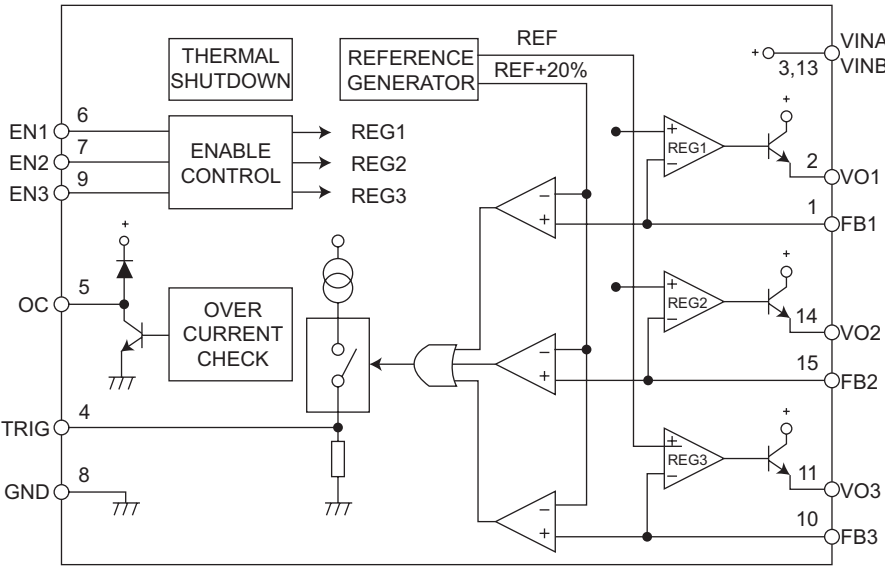
3. Pin functions

Pin No.	Symbol	Function
1	FB1	REG1 feedback voltage input
2	VO1	REG1 output voltage
3	VINA	Input DC supply voltage
4	TRIG	Trigger for external SCR (crowbar protection)
5	OC	Over current warning output
6	EN1	REG1 enable input
7	EN2	REG2 enable input
8	GND	Analog ground
9	EN3	REG3 enable input
10	FB3	REG3 feedback voltage input
11	VO3	REG3 output voltage
12	N.C.	Not connected
13	VINB	Input DC supply voltage
14	VO2	REG2 output voltage
15	FB2	REG2 feedback voltage input

■ LA73054-X (IC601) : Video Driver

1. Pin layout

Top pins (left to right): 36, 35, 34, 33, 32, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19

Top pin labels:
- 36: AMP-1.SW
- 35: DRIVE-1.SW
- 34: VOC21
- 33: COMPOSITE-OUT
- 32: GND21
- 31: CHROMA.OUT
- 30: C_DC.OUT
- 29: GND22
- 28: Y-1.OUT
- 27: GND23
- 26: GND24
- 25: Y-2.OUT
- 24: VCC22
- 23: CB.OUT
- 22: GND25
- 21: CR.OUT
- 20: GND26
- 19: DRIVE-2.SW

Bottom pin labels:
- 1: VOC1
- 2: COMPOSITE.IN
- 3: SQUEEZE.SW
- 4: LETTER-BOX-SW
- 5: MUTE-1.SW
- 6: CHROMA.IN
- 7: GND11
- 8: Y-1.IN
- 9: YC-MIX.SW
- 10: RGB.SW
- 11: Y-2.IN
- 12: MUTE-2.SW
- 13: LPF.SW
- 14: CB.IN
- 15: AMP-2.SW
- 16: CR.IN
- 17: GND12
- 18: REG

Bottom pins (left to right): 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18

2. Block diagram

UX-A10DVD

■ LC75345M-X (IC311) : Function Vol

1. Pin layout
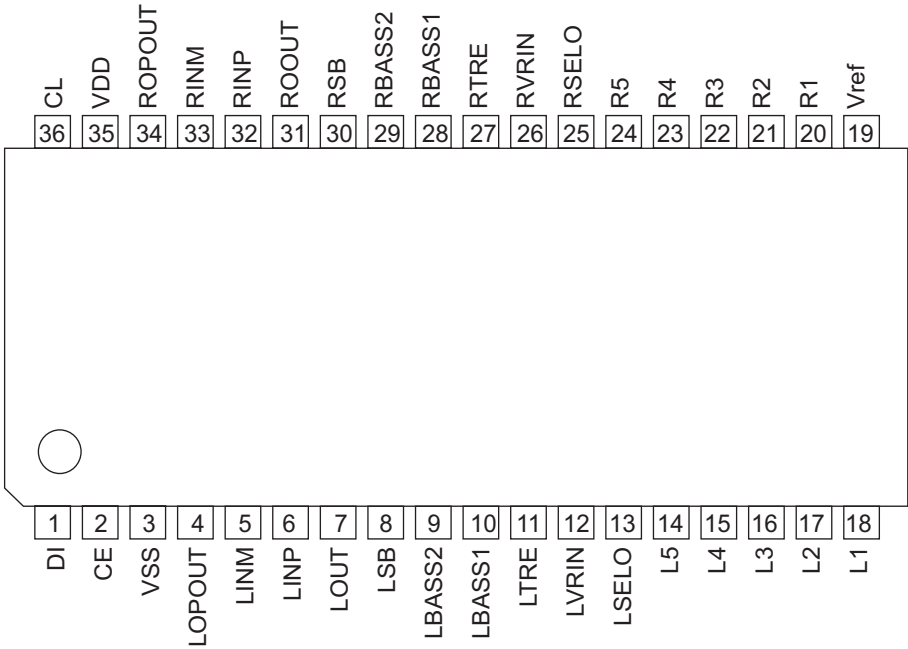
2. Block diagram
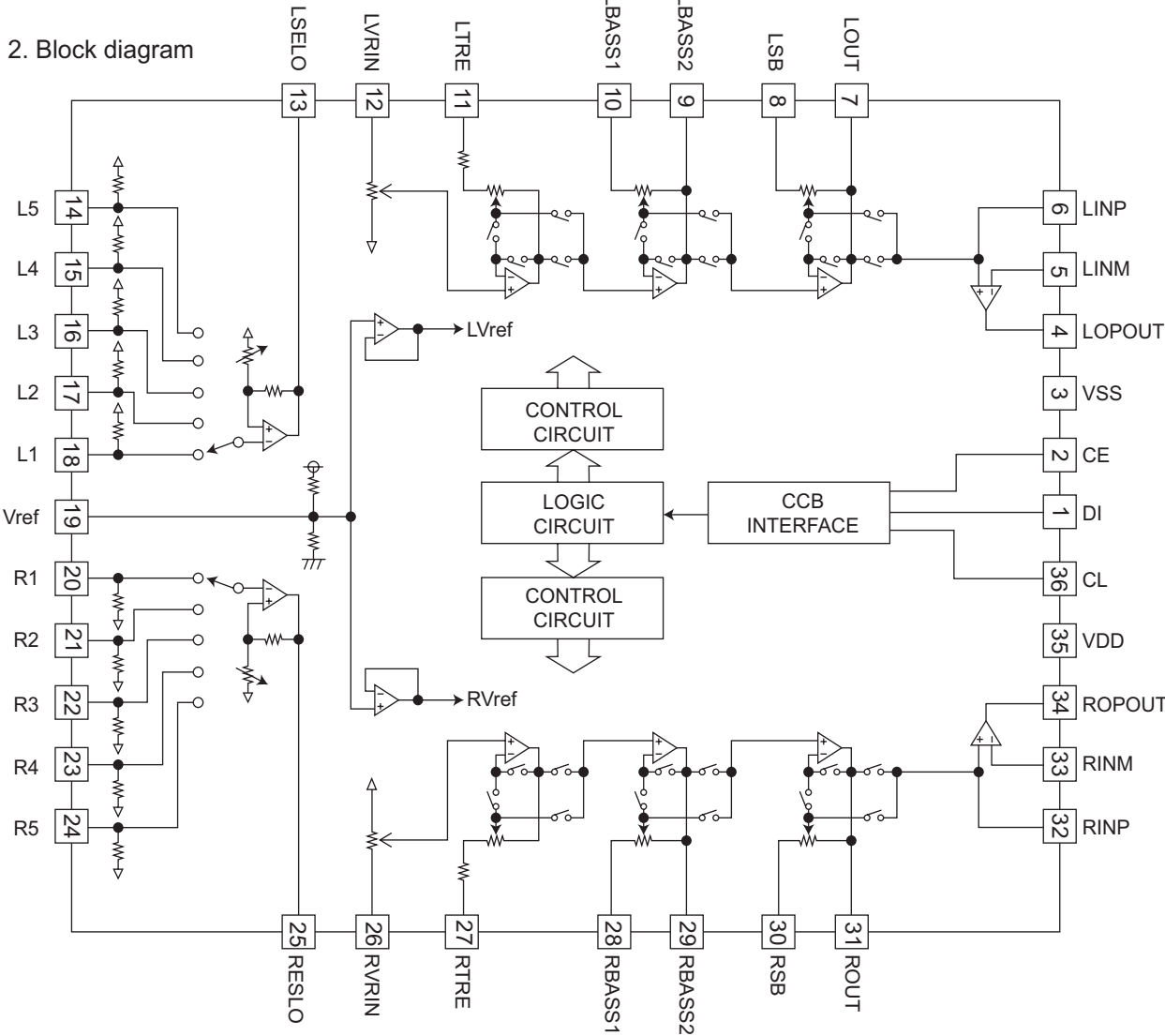
3. Pin function

Pin No.	Symbol	Function
1	DI	Serial data and clock input pin for control.
2	CE	Chip enable pin.
3	VSS	Ground pin.
4	LOPOUT	Output pin of general-purpose operation amplifier.
5	LINM	Non-inverted input pin of general-purpuse operation amplifier.
6	LINP	Non-inverted input pin of general-purpuse operation amplifier.
7	LOUT	ATT + equalizer output pin.
8	LSB	Capacitor and resistor connection pin comprising filters for bass and super-bass band.
9	LBASS2	Capacitor and resistor connection pin comprising filters for bass and super-bass band.
10	LBASS1	Capacitor and resistor connection pin comprising filters for bass and super-bass band.
11	LTRE	Capacitor and resistor connection pin comprising treble band filter.
12	LVRIN	Volume input pin.
13	LSELO	Input selector output pin.
14	L5	Input signal pin.
15	L4	Input signal pin.
16	L3	Input signal pin.
17	L2	Input signal pin.
18	L1	Input signal pin.
19	Vref	0.5 x VDD voltage generation block for analog ground.
20	R1	Input signal pin.
21	R2	Input signal pin.
22	R3	Input signal pin.
23	R4	Input signal pin.
24	R5	Input signal pin.
25	RSELO	Input selector output pin.
26	RVRIN	Volume input pin.
27	RTRE	Capacitor connection pin comprising treble band filter.
28	RBASS1	Capacitor and resistor connection pin comprising filter for bass and super-bass band.
29	RBASS2	Capacitor and resistor connection pin comprising filter for bass and super-bass band.
30	RSB	Capacitor and resistor connection pin comprising filter for bass and super-bass band.
31	ROUT	ATT + equalizer output pin.
32	RINP	Non inverted input pin of general-purpose operation amplifier.
33	RINM	Non inverted input pin of general purpose operation amplifier.
34	ROPOUT	Output pin of general-purpose operation amplifier.
35	VDD	Supply pin.
36	CL	Serial data and clock input pin for control.

UX-A10DVD

■ LB1641 (IC741) : DC Motor driver

1. Pin layout

1	2	3	4	5	6	7	8	9	10
GND	OUT1	P1	VZ	IN1	IN2	VCC1	VCC2	P2	OUT2
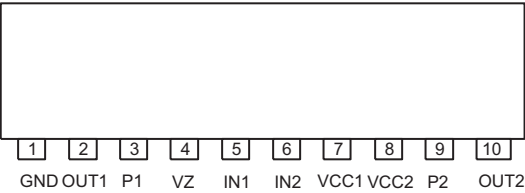
2. Pin function

Input		Output		Mode
IN1	IN2	OUT1	OUT2	
0	0	0	0	Brake
1	0	1	0	CLOCKWISE
0	1	0	1	COUNTER-CLOCKWISE
1	1	0	0	Brake

■ M63008FP-X (IC410) : BTL driver

1.Pin layout

2.Block diagram

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■ MN101C49GKY (IC511) : System Micom

1.Pin layout

Top pins (left to right): P74/A12, P73/A11, P72/A10, P71/A9, P70/A8, P67/A7, P66/A6, P65/A5, P64/A4, P63/A3, P62/A2, P61/A1, P60/A0, P54/A17, P53/A16, P52/NCS, P51/NRE, P50/NWE, P47/KEY7, P46/KEY6, P45/KEY5, P44/KEY4, P43/KEY3, P42/KEY2, P41/KEY1

Top pin numbers (left to right): 75, 74, 73, 72, 71, 70, 69, 68, 67, 66, 65, 64, 63, 62, 61, 60, 59, 58, 57, 56, 55, 54, 53, 52, 51

Left side:
Pin	Number
P75/A13	76
P76/A14	77
P77/A15	78
P80/LED0,D0	79
P81/LED1,D1	80
P82/LED2,D2	81
P83/LED3,D3	82
P84/LED4,D4	83
P85/LED5,D5	84
P86/LED6,D6	85
P87/LED7,D7	86
PD0/SD00	87
PD1/SD01	88
PD2/SD02	89
PD3/SD03	90
PD4/SD04	91
PD5/SD05	92
PD6/SD06	93
PD7/SD07	94
DAVSS	95
PC0/DA0	96
PC1/DA1	97
PC2/DA2	98
PC3/DA3	99
DAVDD	100

Right side:
Number	Pin
50	KEYO/P40
49	NDKDMA/P37
48	NSTDMA/P36
47	SBT3/SCL/NLDDMA/P35
46	SBI3/NBT/P34
45	SBO3/SDA/NBR/P33
44	SBT1/P32
43	SBT1/RXD1/P31
42	SBO1/TXD1/P30
41	P17
40	TM4IO/P16
39	P15
38	TM7IO/P14
37	TM3IO/P13
36	TM2IO/P12
35	TM1IO/P11
34	RMOUT/TM0IO/P10
33	NRST/P27
32	P26
31	IRQ5/P25
30	IRQ4/P24
29	IRQ3/P23
28	IRQ2/P22
27	ACZ/IRQ1/P21
26	IRQO/P20

Bottom pin numbers (left to right): 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25

Bottom pins (left to right): VREF-, AN0/PA0, AN1/PA1, AN2/PA2, AM3/PA3, AM4/PA4, AM5/PA5, AM6/PA6, AM7/PA7, VREF+, VDD, OSC2, OSC1, VSS, XI, XO, MMOD, POO/TXDO/SBOOPO, 1/RXDO/SBIO, PO2/SBTO, SBO2/PO3, SBI2/PO4, SBT2/PO5, NDK/BUZZER/PO6, SYSCLK/PO7

■ MN102L62GMA1 (IC401) : Unit CPU

1.Pin layout

Top pins (left to right): NMI, *, *, SBO1,P75, SBT1,P74, SBT1,P73, SBO0,P72, SBT0,P71, SBT0,P70, VDD, AN3,P97, AN2,P96, AN1,P95, AN0,P94, VSS, TM7IC,P93, TM7IOB,P92, TM7IOA,P91, TM6IC,P90, TM6IOB,P87, TM6IOA,P86, VDD, TM5IO,P85, TM4IO,P84, TM3IO,P83

Left side:
Pin	Number
PA0,IRQ0	75
PA1,IRQ1	76
PA2,IRQ2	
PA3,IRQ3	
PA4,IRQ4	
PAS,ADSEP	
RST	
VDD	
P00,D00,AD00	
P01,D01,AD01	
P02,D02,AD02	
P03,D03,AD03	
P04,D04,AD04	
P05,D05,AD05	
P06,D06,AD06	
P07,D07,AD07	
VSS	
P10,D08,AD08	
P11,D09,AD09	
P12,D10,AD10	
P13,D11,AD11	
P14,D12,AD12	
P15,D13,AD13	100
P16,D14,AD14	
P17,D15,AD15	1

Right side:
Number	Pin
51	TM2IO,P82
50	TM1IO,P81
	TM0IO,P80
	A23,WDOUT,AN7,P47
	A22,STOP,AN6,P46
	A21,AN5,P45
	A20,AN4,P44
	VSS
	A19,P43
	A16,P42
	A17,P41
	A16,P40
	A15,P37
	A14,P36
	A13,P35
	A12,P34
	VDD
	A11,P33
	A10,P32
	A09,P31
	A08,P30
	A07,P27
26	A06,P26
	A05,P25
25	A04,P24

Bottom pins (left to right): P60,WAIT, P61,RE, P62,WEL, P63,WEH, P50,CS0, P51,CS1, P52,CS2, P53,CS3, P54,BREQ, P55,BRACK, P56,ALE,ALE,BSTRE, P57,WORD, P20,A00, P21,A01, P22,A02, P23,A03, VDD, SYSCLK, Vss, XI, XO, VDD, OSCI, OSCO, MODE

■ MN103S28EGA (IC301) : SODC

1.Pin layout

Top pins (176 to 133):
MASTER, NRESET, VDD3, HDD7, HDD8, HDD6, VSS, VDD3, HDD9, HDD5, HDD10, HDD4, HDD11, VSS, VDD3, HDD3, HDD12, HDD2, HDD13, HDD1, VDD3, VSS, UATASEL, P0, VDD18, HDD14, HDD0, HDD15, DMARQ, NIOWR, NIORD, IORDY, VSS, VDD3, NDMACK, INTRQ, NIOCS15, DA1, NPDJAG, DA0, DA2, NCS1FX, NCS3FX, NDASP

Left pins (1 to 44):
NINT0, NINT1, VDD3, VSS, NINT2, WAITODC, NMRST, DASPST, CPUADR17, CPUADR16, CPUADR15, CPUADR14, CPUADR13, CPUADR12, CPUADR11, CPUADR10, CPUADR9, VDD18, VSS, DRAMVDD18, DRAMVSS, CPUADR8, CPUADR7, CPUADR6, CPUADR5, CPUADR4, CPUADR3, CPUADR2, CPUADR1, CPUADR0, VDD3, VSS, DRAMVDD33, NCS, NWR, NRD, CPUDT7, CPUDT6, CPUDT5, CPUDT4, CPUDT3, CPUDT2, CPUDT1, CPUDT0

Right pins (132 to 89):
NTRYCL, NEJECT, MONI3, MONI2, MONI1, MONI0, VSS, VDD3, TECAPA, AD6/CAPAC1, AD5/CAPAC2, AD4, AD3, AD2, AD1, AD0, AVDD, DAC1, DAC0, AVSS, JITOUT, ARF, NARF, AVDD, DSLF1, DSLF2, VHALF, PLPG, VREFH, RVI, AVSS, PLFLT1, PLFLT2, AVDD, RFDIF, CSLFLT, HPFIN, HPFOUT, AVSS, LPFIN, LPFOUT, CMPIN, TRCRS, VCOF

Bottom pins (45 to 88):
CLKOUT1, MMOD, NRST, MSTPOL, SCLOCK, SDATA, OFTR, BOO, PWM1, PWM2, PWM3, PWM4, VDD3, DRAMVDD18, DRAMVSS, VSS, PWM5, PWM6, PWM7, PWM8, TBAL, FBAL, TRSDRV, SPDRV, FG, TILTP, TILT, TILTN, TX, DTRD, IDGT/TEMUTE, VDD18, VSS, VDD3, OSCI1, OSCO1, VSS, TSTSG, VFOSHORT, JLINE, AVSS, ROUT, LOUT, AVDD

Corner labels: 176, 133, 132, 1, 44, 45, 89, 88

■ MN35505-X (IC202) : D/A Converter

1.Pin layout

1.Block diagram

3.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	M5	I	Connects with VDD	15	AVSS2	-	Analog playground 2
2	DIN	I	Data input	16	OUT2D	O	2D PEM output
3	LRCK	I	L/RClock input	17	AVDD2	-	Analog power supply 2
4	BCK	I	Bit clock input	18	OUT2C	O	2C PEM output
5	M3	I	Connects with playground	19	M9	I	NC
6	DVDD2	-	Digital power supply 2	20	DVSS1	-	Digital grand pin 1
7	CKO	I	NC	21	XOUT	O	Crystal oscillator output
8	DVSS2	-	Digital ground 2	22	XIN	I	Crystal oscillator input
9	M2	I	Connects with playground	23	VCOF	I	VCO Filter
10	M1	I	Connects with playground	24	DVDD1	-	Digital power supply 1
11	OUT1C	O	1C PEM output	25	M7	I	System clock rate selection
12	AVDD1	-	Analog power supply 1	26	M8	I	System clock rate selection
13	OUT1D	O	1d PEM output	27	M4	I	Reset signal
14	AVSS1	-	Analog playground 1	28	M6	I	Connects with VDD

UX-A10DVD

■ MR27V1602EUMTPX (IC402) : 16M ROM

1.Pin layout

2.Block diagram

16When 8- bit is output, these pins
are in the state of high impedance.
The D15 pin functions as A-1.
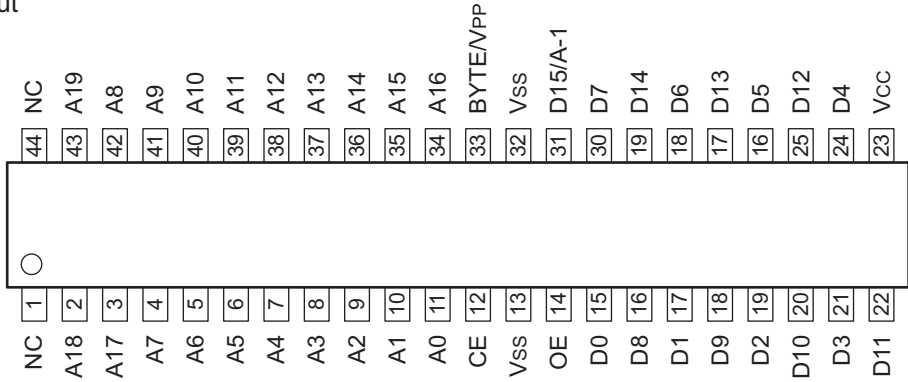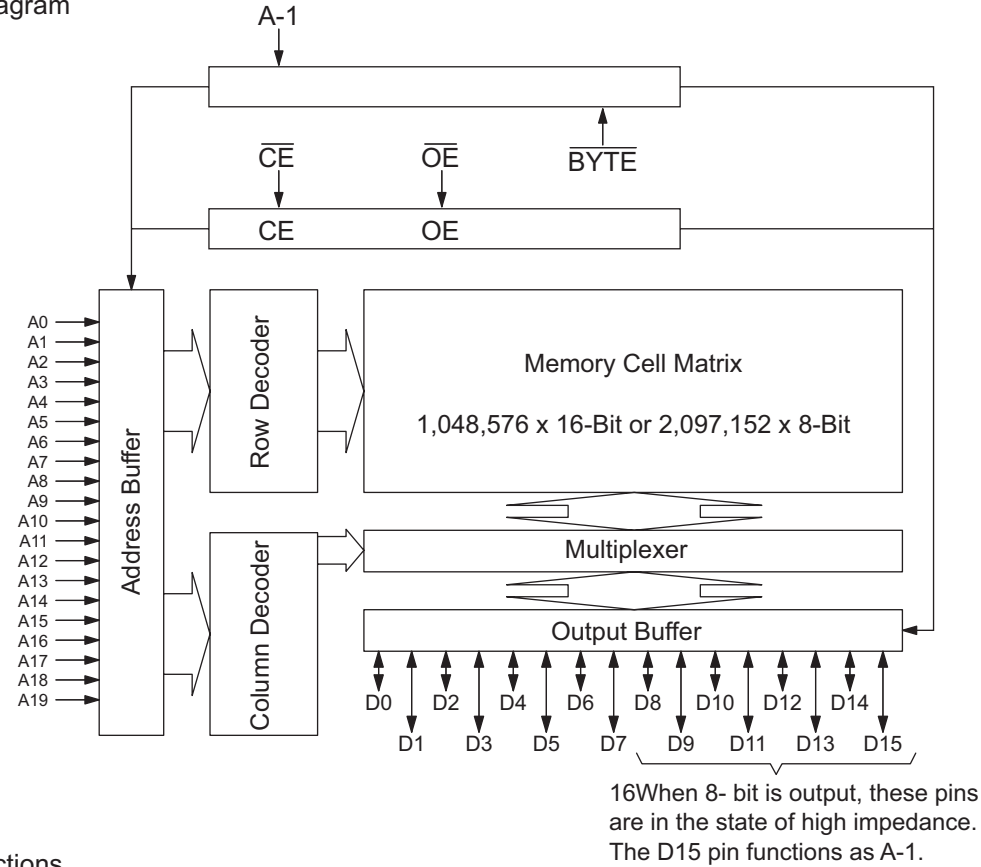
3.Pin Functions

Pin No,	Symbol	Function
1	NC	No connection
2~11	A18,A17,A7~A0	Address input
12	CE	Chip enable
13	VSS	GND
14	OE	Output enable
15~22	D0,D8,D1,D9,D2, D10,D3,D11	Data output
23	VCC	Power supply
24~30	D4,D12,D5,D13, D6,D14,D7	Data output
31	D15/A-1	Data output / Address input
32	VSS	GND
33	BYTE/VPP	Mode Switch
34~43	A16~A8,A19	Address input
44	NC	No connection

■ NJM4580M-X (IC211) : Dual operational amplifier

1.Pin layout

A OUT | 1 | | 8 | V+
A -IN | 2 | A | 7 | B OUT
A +IN | 3 | B | 6 | B -IN
V- | 4 | | 5 | B +IN

2.Block diagram

V+

INPUT − +

OUTPUT

V-
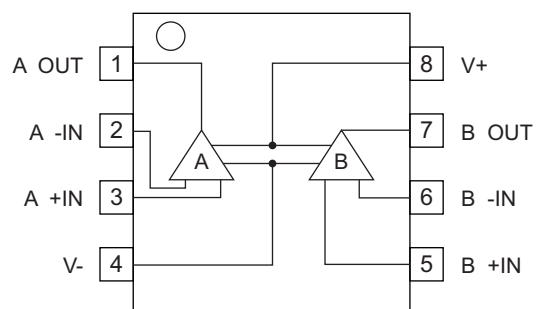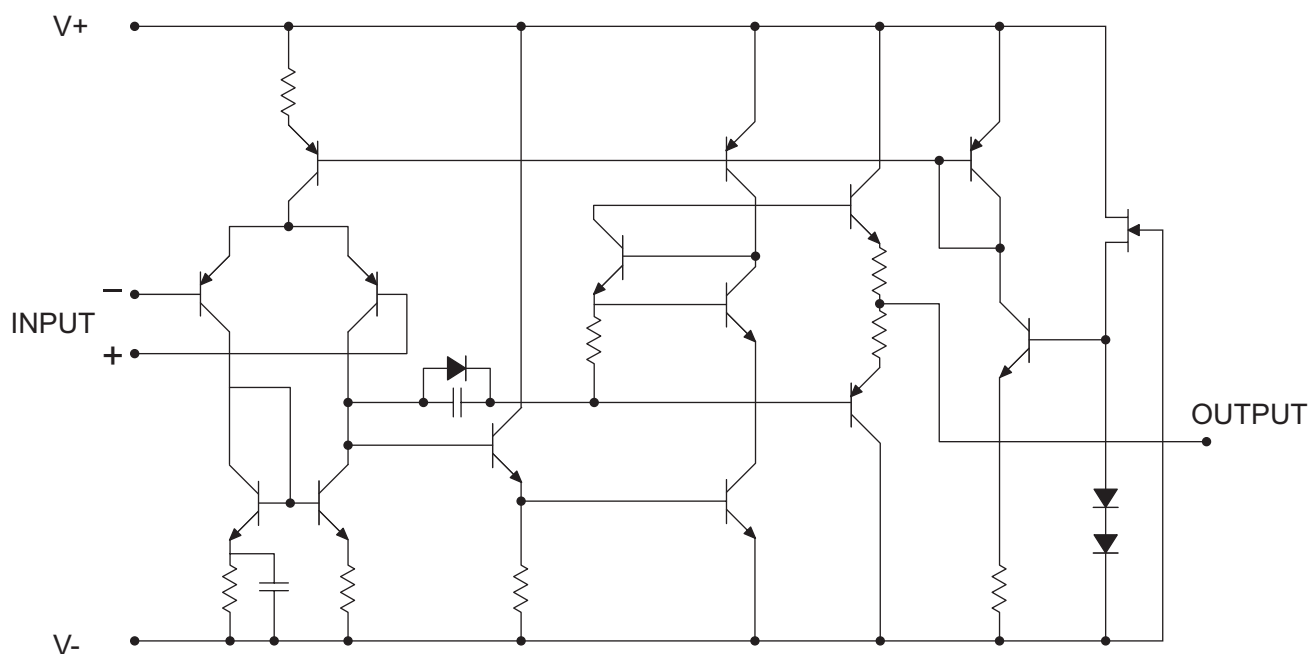
■ SG-105F3-BB.C(IC1) : Reel pulse

1.Pin layout / Block diagram
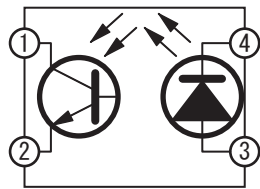
■ TC74HCU04AF-W (IC393) : Inverter

1.Pin layout
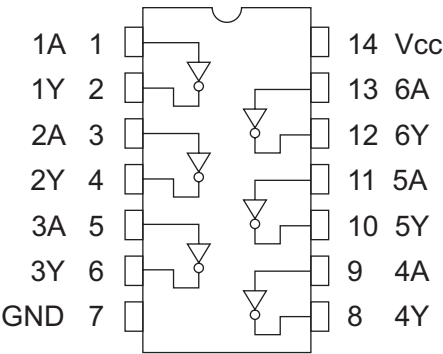
2.Truth table

A	Y
L	H
H	L

■ TC7S08F-W (IC340) : APC PWM Buffer

1. Pin layout
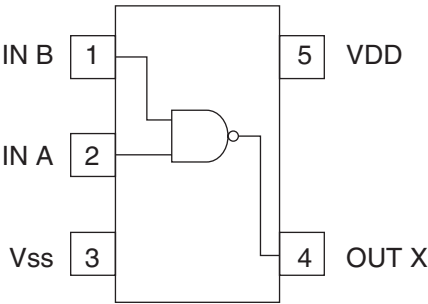
2. Block diagram
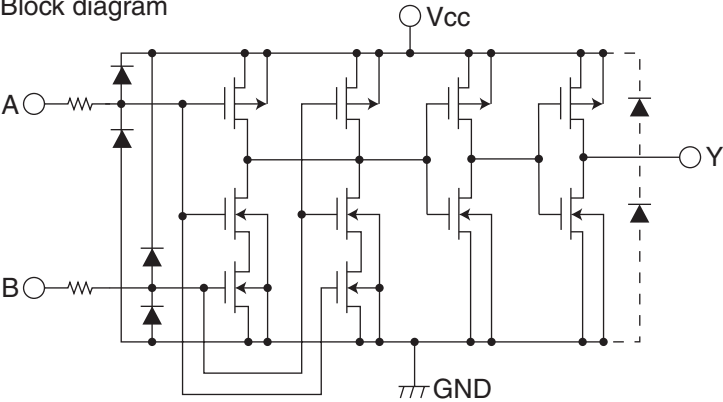
■ STK402-050 (IC111) : Power amp.

1.Pin layout

1 ~ 15

2.Block diagra

UX-A10DVD
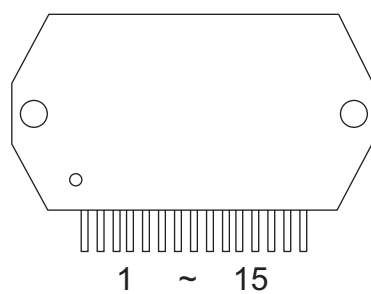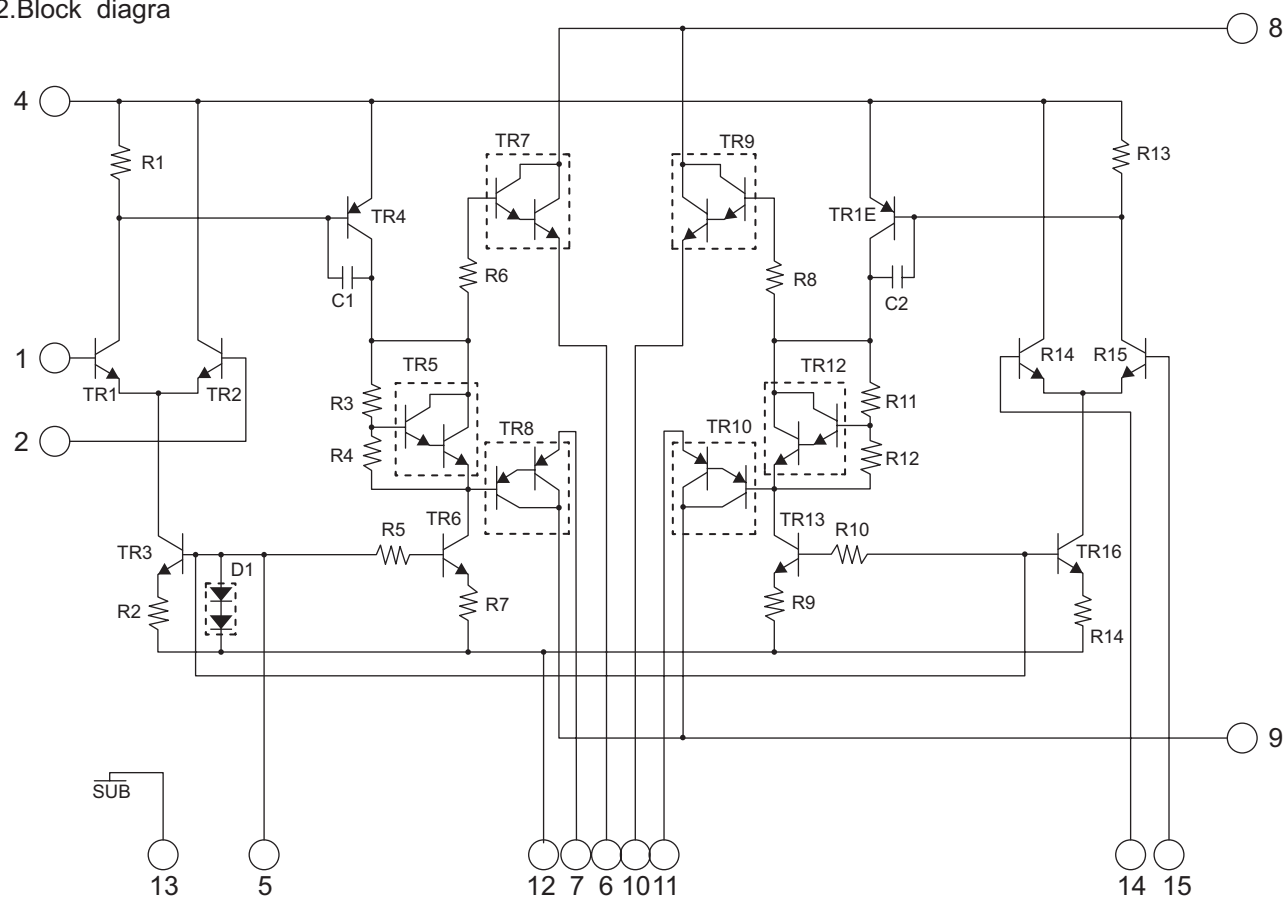
■ UPD784217AGC174 (IC500) : CPU

1. Pin layout

```
         75   ~   51
    76 ┌─────────────┐ 50
       │             │
     ~ │             │ ~
   100 │             │ 26
       └─────────────┘
          1   ~   25
```
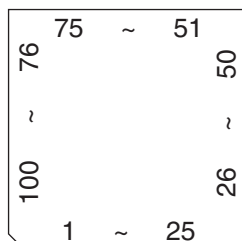
2. Pin function (1/2)

Pin No.	Symbol	I/O	Function
1～5	NC	-	Non connect
6	CD-MUTE	O	CD MUTE
7	CD-REST	O	CD REST
8	ANT REM	O	Antenna remote output
9	VDD	-	5V connection
10	X2	-	Connect to X'tal for main clock
11	X1	-	Connect to X'tal for main clock
12	VSS	-	Connect to GND
13	XT2	-	Connect to X'tal for sub clock
14	XT1	-	Connect to X'tal for sub clock
15	RESET	I	Reset detection terminal
16	P.REQ	O	Mechanism power supply ON/OFF demand output ("L" on demand)
17	BUS-INT	I	J-BUS signal interrupt input
18	PS2	I	Power save 2
19	NC	-	Non connect
20	RDS-SCK	I	Clock input for RDS
21	RDS-DA	I	RDS data input
22	REMOCON	I	Remocon signal input
23	AVDD	I	5V connect
24	AVREF0	I	5V connect
25	SD/ST	I	Station detector, Stereo signal input
26	MRC DATA	I	MRC data input
27	KEY0	I	Key input 0
28	KEY1	-	Key input 1
29	TEMP	I	Temperature data input for contrast correction
30	LEVEL	-	Level meter input
31	SQ	I	S.quality level input
32	SM	-	S.meter level input
33	AVSS	-	Connect to GND
34	INLOCK	I	Lock detection output
35	NC	O	Non connect
36	AVREF	I/O	5V connect
37	BUS-SI	I	J-BUS data input
38	BUS-SO	O	J-BUS data output
39	BUS-SCK	O	J-BUS clock input/output
40	LCD-CE1	O	Chip enable 1 out put for LCD driver
41	LCD-DA	O	Data output for LCD driver
42	LCD-CL	O	Clock output to LCD driver
43	LCD-CE2	O	Chip enable 2 out put for LCD driver
44	BUZZER	O	Buzzer output
45	EPDAI	I	Communication data input 12C

2. Pin function (2/2) UPD784217AGC174

Pin No.	Symbol	I/O	Function
46	EP-DAO	O	Communication data input of 12C
47	EPCLK	O	Communication data input of 12C
48	BUS-I/O	O	J-BUS I/O switching output
49	PM0	O	Panel close side motor control signal output
50	PM1	O	Panel open side motor control signal output
51	EQ-CLK	O	Equalizer clock
52	EQ-DA	O	Equalizer data
53	EQ-LA	O	Equalizer latch
54	STAGE	I	H:L: Initialization port
55	VCR CONT	O	VCR control signal output
56~61	PNL-SW1~6	I	Panel position detection switch 1 to 6 signal input
62	NC	-	Non connect
63	NC	-	Non connect
64	NC	-	Non connect
65	FM/AM	O	FM / AM select output
66	PLL-CE	O	PLL IC control CE output
67	PLL-DO	O	PLL IC control data output
68	PLL-CLK	O	PLL IC control clock output
69	PLL-DI	I	PLL IC control data input
70	NC	-	Non connect
71	TELMUTE	I	Telephone mute signal detection input
72	VSS	-	Connect to GND
73	DIM-IN	I	Dimmer detection input
74	PS1	I	Power save 1
75	POWER	O	Power ON / OFF select output
76	CD-ON	O	CD power supply control signal output
77	MUTE	O	Mute output
78	W-LPF1	O	Sub woofer cut off frequency control output 1
79	W-LPF2	O	Sub woofer cut off frequency control output 2
80	W-MUTE	O	Sub woofer mute output
81	VDD	O	5V connect
82	VOL-DA	O	E. volume IC control data output
83	VOL-CLK	O	E. volume IC control clock data output
84	CF SEL	O	FM band area filter select signal output
85	PMKICK	O	Panel motor kick signal output
86	NC	-	Non connect
87	NC	-	Non connect
88	VOL-1	I	Rotary volume pulse
89	VOL-2	I	Rotary volume pulse signal input
90	J/U	I	Pull down
91	NC	-	Non connect
92	NC	-	Non connect
93	NC	-	Non connect
94	TEST	I/O	Connect to GND
95	NC	-	Non connect
96	NC	-	Non connect
97	NC	-	Non connect
98	NC	-	Non connect
99	DISCSEL	O	H: 8 cm disc non correspondence L: 8 cm disc correspondence
100	NC	-	Non connect

■ UPD784217AGF525 (IC701) : System CPU

1.Pin layout

```
○ 100   ~    81
 1                  80

 ⸾                  ⸾

 30                 51
      31   ~   50
```
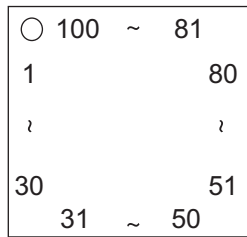
2.Pin Functions   1/2

Pin No.	Symbol	I/O	Function
1	POUTRELAY	O	Main transformer relay CTL
2	POUTFL	O	Power supply control of FL driver
3	MDRESET	O	MD Reset
4	NC	O	Unused
5	FANON	O	Fan control
6	NC	-	Unused
7	PROTECT	I	Speaker output abnormality detection
8	HPMUTE	O	Headphone mute
9	VDD	-	Digital power supply
10	PMT0	O	Panel motor control
11	PMT1	O	Panel motor control
12	RMSPEED	O	Panel motor speed control(always "L" output)
13	FDVD	O	DVD unit power supply control
14	POUTMDAMP	O	REG IC MD6V
15	NC	-	Unused
16	VOLCE	O	CE of volume IC
17	VOLDATA	O	Data of volume IC
18	AHB	O	Actively hyper bus
19	POUTPAMP	O	Enable contororl of power amplifier
20	SMUTE	O	System mute
21	DVDTRAY	O	Power supply control for DVD tray
22	TEST(VPP)	-	Test (power supply)
23	PANEL_SW1	I	Panel switch
24	NC	-	Unused
25	PANEL_SW3	I	Panel switch
26	PANEL_SW4	I	Panel switch
27,28	NC	-	Unused
29	PIN	I	Power key
30	JOGL	I	Jog input
31	JOGR	I	Jog input
32	LEDCTL(STBY)	O	Standby LED
33	VOLCK	O	Clock of volume IC
34	BUP	I	Power failure detection
35	+BCTL	O	Power supply control
36	XKIL	O	Sub-clock stop control
37	VDD	-	Digital power supply
38	X2	-	Main clock connection
39	X1	I	Main clock connection
40	VSS	-	Digital playground
41	XT2	-	Sub-clock connection
42	XT1	I	Sub-clock connection
43	RESET	I	Reset terminal and L active of this microcomputer
44	REM	I	Remote control input
45	RDS_CK	I	RDS clock input
	NC	-	Unused
46	S2MREQ	I	BUSY from sub-microcomputer
47	PHOTO	I	Reel pulse detection

2.Pin Functions   2/2

Pin No.	Symbol	I/O	Function
48	LOCK	I	Abnormal detection of panel
49	NC	-	Unused
50	RDS_ST	O	RDS *stororb*
	NC	-	Unused
51	AVDD	-	A/D and D/A digital power supply
52	AVREF0	I	A/D and D/A converter
53	SAFETY4	I	Abnormal detection of MD6V power supply
	NC	-	Unused
54	SAFETY3	I	Abnormal detection of SW10V, DVDM9V, and DVD5V
55	SAFETY5	I	Abnormal detection of DVD3 and 3V power supply
56	KEY1	I	Tape relation detection
57	VERSION	I	Version (destination) detection
58	FKEY2	I	Key detection
59	FKEY1	I	Key detection
60	SAFETY1	I	Abnormality of voltage of solenoid in cassette mechanism SLC detection
61	AVSS	-	A/D and D/A digital playground
62	ECHO1	O	Echo adjustment
63	ECHO2	O	Echo adjustment
64	AVREF1	I	A/D and D/A converter
65	MDSTAT	I	Status from MD unit
	NC	-	Unused
66	MDCMD	O	Command to MD unit
	NC	-	Unused
67	MICIN	I	MIC detection
68	S2MDATA	I	Data from sub-microcomputer to the main microcomputer
69	M2SDATA	O	Data from the main microcomputer to sub-microcomputer
70	M2SCLK	O	Cereal lock of sub-microcomputer and the main microcomputer
71	M2SREQ	O	Data request to sub-microcomputer
72	SMON	O	Sub-microcomputer power supply control
73	NC	-	Unused
74	FLDATA	O	FL driver CTL
75	FLCLK	O	FL driver CTL
76	STTA	O	TAPE module control
77	SDATA	O	TAPE module control
78	SCK	O	TAPE module control
79	PLAY	I	TAPE module
80	SPKRELAY	O	Speaker relay
81	TUDATA_IN	I	Data from tuner
82	TUDATA_OUT	O	Data to tuner
83	TUCLK	O	Clock to tuner
84	TUCE	O	CE to tuner
85	RDS_DT	I/O	RDS data
	NC	-	Unused
86	FTU	O	Tuner power supply
87	NC	-	Unused
88	POUTLOG	O	Power supply control of logic of FL
89	FLSTB	O	FL driver CTL
90	FLBK	O	FL driver CTL
91	CRED	O	Panel LED
92	RGREEN	O	Panel LED
93	RBLUE	O	Panel LED
94	RRED	O	Panel LED
95	LGREEN	O	Panel LED
96	LBLUE	O	Panel LED
97	LRED	O	Panel LED
98	CGREEN	O	Panel LED
99	CBLUE	O	Panel LED
100	VSS	-	Digital playground

■ ZIVA-4.1-PBO (IC501) : AV decoder

1.Pin layout

Top pins (left to right): VDD_RREF, RREF, VSS_RREF, VDD_VIDEO, VDD_DAC, C/RV, VSS_VIDEO, VSS_DAC, NC, VDD_VIDEO, VDD_DAC, Y/B/U, VSS_VIDEO, VSS_DAC, NC, VDD_VIDEO, VDD_DAC, CVBS/G/Y, VSS_VIDEO, VSS_DAC, NC, VDD_VIDEO, VDD_DAC, CVBS, VSS_VIDEO, VSS_DAC, NC, VSS, VDD_2.5, DA-IEC, DA-BCK, DA-XCK, VSS, VDD_3.3, DA-LRCK, DA-DATA0, DA-DATA1, DA-DATA2, DA-DATA3, DAI-DATA, VSS, VDD_3.3, DAI-BCK, DAI-LRCK, RESERVED, RESERVED, RESERVED, NC, RESERVED, NC, RESERVED

Left pins (top to bottom): A_VSS, SYSCLK, VCLK, A_VDD, DVD-DATA0/CD-DATA, DVD-DATA1/CD-LRCK, DVD-DATA2/CD-BCK, DVD-DATA3/CD-C2P0, DVD-DATA4/CDG-SDATA, VSS, VDD_3.3, DVD-DATA5/CDG-VFSY, DVD-DATA6/CDG-SOS1, DVD-DATA7/CDG-SCLK, VDACK, VREQUEST, VSTROBE, ERROR, VDD_3.3, RESERVED, VDD_3.3, VSS, NC, RESERVED, NC, HADDR0, HADDR1, HADDR2, RESERVED, RESERVED, RESERVED, VSS, VDD_2.5, RESERVED, VSS, VDD_3.3, RESERVED, RESERVED, RESERVED, RESERVED, HDATA7, VSS, HDATA6, HDATA5, HDATA4, HDATA3, HDATA2, VDD_3.3, VSS, HDATA1, HDATA0, CS

Right pins (top to bottom): MADDR3, MADDR2, MADDR1, VSS, VDD_3.3, MADDR0, MADDR10, SD-BS, SD-CS1/MADDR11, SD-CS0, SD-RAS, VSS, VDD_3.3, SD-CAS, MWE, MADDR4, VSS, VDD_2.5, MADDR5, MADDR6, MADDR7, VSS, VDD_3.3, MADDR8, MADDR9, CLKSEL, SD-CLK, LDQM, MDATA8, VSS, VDD_3.3, MDATA9, MDATA10, MDATA11, MDATA12, MDATA13, VSS, VDD_2.5, MDATA14, VSS, VDD_3.3, MDATA15, MDATA7, MDATA6, MDATA5, MDATA4, MDATA3, MDATA2, VSS, VDD_3.3, MDATA1, MDATA0

Bottom pins (left to right): RD, R/W, VDD_3.3, WAIT, RESET, VSS, VDD_3.3, INT, NC, NC, NC, NC, VDD_2.5, VSS, NC, NC, NC, NC, VSS, VDD_3.3, VDATA0, VDATA1, VDATA2, VDATA3, VDATA4, VDATA5, VDATA6, VDATA7, VSYNC, HSYNC, VSS, VDD_3.3, NC, NC, NC, VDD_2.5, VSS, NC, NC, NC, NC, VSS, VDD_3.3, PIO0, PIO1, PIO2, PIO3, PIO4, PIO5, PIO6, PIO7

Corner markers: 156, 157, 105, 104, 208, 1, 53, 52

2.Pin function   1/4

Pin No.	Symbol	I/O	Function
1	RD	I	Read strobe in I mode.Must be held HIGH in M mode.
2	R/W	I	Read/write strobe in M mode. Write strobe in I mode.Host asserts R/WLOW to select Write and LOW to select Read for M mode only.
3	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
4	WAIT	O,OD,PU	Transfer not complete / data acknowledge.Active LOW to indicate host initiated transfer is not complete.WAIT is asserted after the falling edge of CS and reasserted when decoder is ready to complete transfer cycle.Open drain signal,must be pulled-up via 1kΩ to 3.3 volts.Driven high for 10 ns before tristate.
5	RESET	I	Active Low Reset.Assert for at least 5-milliseconds in the presence of clock to reset the entire chip
6	VSS	Ground	Ground for core logic and I/O signals
7	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
8	INT	O,OD,PU	Host interrupt.Open drain signal,must be pulled-up via 4.7kΩ to 3.3 volts.
9~12	NC	O	No connect
13	VDD_2.5	Power	2.5-V supply voltage for core logic
14	VSS	Ground	Ground for core logic and I/O signals
15~18	NC	O	No connect
19	VSS	Ground	Ground for core logic and I/O signals
20	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
21~28	VDATA0~7	O	Video data bus.Byteserial CbYCrY data synchronous with VCLK.At power-up,the decoder does not drive VDATA.During boot-up,the decoder uses configuration parameters to drive or 3-state VDATA.
29	VSYNC	I/O	Vertical sync.Bi-directional,the decoder outputs the top border of a new field on the first HSYNC after the falling edge of VSYNC,VSYNC can accept vertical synchronization or top/bottom field notification from an external source. (VSYNC HIGH=bottom field.VSYNC LOW=Top field)

2.Pin function   2/4

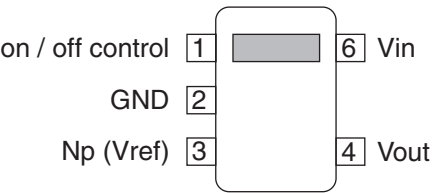| Pin No.	Symbol	I/O	Function
30	HSYNC	I/O	Horizontal sync.The decoder begins outputting pixel data for a new horizontal line after the falling(active)edge of HSYNC.
31	VSS	Ground	Ground for core logic and I/O signals
32	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
33~35	NC	O	No connect
36	VDD_2.5	Power	2.5-V supply voltage for core logic
37	VSS	Ground	Ground for core logic and I/O signals
38~42	NC	O	No connect
43	PIO0	I/O	Programmable I/O pins.
44	VSS	Ground	Ground for core logic and I/O signals
45	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
46~52	PIO1~7	I/O	Programmable I/O pins.
53,54	MDATA0,1	I/O	SDRAM Data
55	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
56	VSS	Ground	Ground for core logic and I/O signals
57~62,63	MDATA2~7,15	I/O	SDRAM Data
64	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
65	VSS	Ground	Ground for core logic and I/O signals
66	MDATA14	I/O	SDRAM Data
67	VDD_2.5	Power	2.5-V supply voltage for core logic
68	VSS	Ground	Ground for core logic and I/O signals
69~73	MDATA13~9	I/O	SDRAM Data
74	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
75	VSS	Ground	Ground for core logic and I/O signals
76	MDATA8	I/O	SDRAM Data
77	LDQM	O	SDRAM Lower or Upper Mask
78	SD-CLK	O	SDRAM Clock
79	CLKSEL	I	Selects SYSCLK or VCLK as clock source.Normal operation is to tie HIGH.
80,81	MADDR9,8	O	SDRAM Address
82	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
83	VSS	Ground	Ground for core logic and I/O signals
84~86	MADDR7~5	O	SDRAM Address
87	VDD_2.5	Power	2.5-V supply voltage for core logic
88	VSS	Ground	Ground for core logic and I/O signals
89	MADDR4	O	SDRAM Address
90	MWE	O	SDRAM Write Enable
91	SD-CAS	O	Active LOW SDRAM Column Address
92	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
93	VSS	Ground	Ground for core logic and I/O signals
94	SD-RAS	O	Active LOW SDRAM Row Address
95	SD-CSO	O	Active LOW SDRAM Chip Select 0
96	SD-CS1 /MADDR11	O	Active LOW SDRAM Chip Select 1 or use as MADDR11 for larger SDRAM (64 Mbits).
97	SD-BS	O	SDRAM Bank Select
98,99	MADDR10,0	O	SDRAM Address
100	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
101	VSS	Ground	Ground for core logic and I/O signals
102~104	MADDR1~3	O	SDRAM Address
105	RESERVED	I	Tie to VSS or VDD_3.3 as specified in Table 1.
106,107	NC	O	No connect
108	RESERVED	I	Tie to VSS or VDD_3.3 as specified in Table 1.
109	NC	O	No connect
110~112	RESERVED	I	Tie to VSS or VDD_3.3 as specified in Table 1.
113	DAI-LRCK	I	PCM left/right clock.
114	DAI-BCK	I	PCM input bit clock.
115	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
116	VSS	Ground	Ground for core logic and I/O signals
117	DAI-DATA	I	PCM data input.
118,121	DA-DATA3~0	O	PCM Data Out.Eight channels.Serial audio samples relative to DA_8CK and DA_LRCK.
122	DA-LRCK	O	PCM Left Clock.Identifies the channel for each sample.The polarity is program mable

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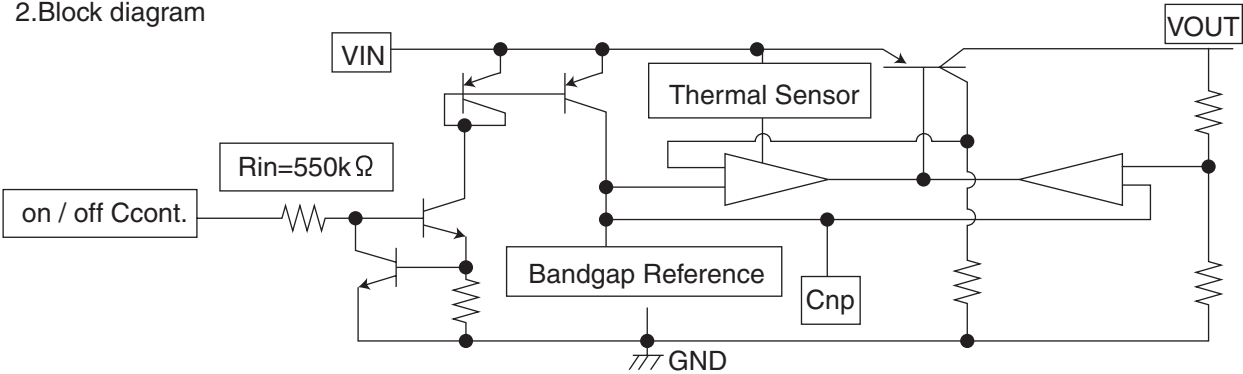| Pin No.	Symbol	I/O	Function
123	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
124	VSS	Ground	Ground for core logic and I/O signals
125	DA-XCK	I/O	Audio External Frequency Clock input or output.DA_8CK and DA_LRCK are derived from this clock.DA_XCK can be 384 or 256 times the sampling frequency
126	DA-BCK	O	PCM Bit Clock.Divided by 8 from DA_XCK.DA_BCK can be either 48 or 32 times the sampling frequency
127	DA-IEC	O	PCM data out in IEC-958 format or compressed data out in IEC-1937 format.
128	VDD_2.5	Power	2.5-V supply voltage for core logic
129	VSS	Ground	Ground for core logic and I/O signals
130	NC	O	No connect.
131	VSS_DAC	Ground	Analog Video DAC Ground
132	VSS_VIDEO	Ground	Analog Video Ground
133	CVBS	Analog O	DAC video output format:CVBS.Macrovision encoded.
134	VDD_DAC	Power	Analog Video DAC Power
135	VDD_VIDEO	Power	3.3-V Analog Video Power
136	NC	O	No connect.
137	VSS_DAC	Ground	Analog Video DAC Ground
138	VSS_VIDEO	Ground	Analog Video Ground
140	VDD_DAC	Power	Analog Video DAC Power
141	VDD_VIDEO	Power	3.3-V Analog Video Power
142	NC	O	No connect.
143	VSS_DAC	Ground	Analog Video DAC Ground
144	VSS_VIDEO	Ground	Analog Video Ground
145	Y/B/U	Analog 0	DAC video output format.Macrovision encoded.
146	VDD_DAC	Power	Analog Video DAC Power
147	VDD_VIDEO	Power	3.3-V Analog Video Power
148	NC	O	No connect.
149	VSS_DAC	Ground	Analog Video DAC Ground
150	VSS_VIDEO	Ground	Analog Video Ground
151	C/R/V	Analog 0	DAC video output format.Macrovision encoded.
152	VDD_DAC	Power	Analog Video DAC Power
153	VDD_VIDEO	Power	3.3-V Analog Video Power
154	VSS_RREF	Ground	Video Analog Ground
155	RREF	Analog 0	Reference Resistor.Connecting to pin 154 through a 1.18k+/.1% resistor is recommended.See on.
156	VDD_RREF	Power	3.3V Analog Video Power
157	A_VSS	Ground	Analog PLL Ground
158	SYSCLK	I	Optional System Clock.Tie to A_VDD through a 1k Ohmresistor
159	VCLK	I	System clock that drives internal PLLs and internal DENC.ZiVA-4.1requires anexternal 27-MHz TTL oscillator.
159	VCLK	I	Video clock.Clocks out data on input.VDATA(7:0).Clock is typically 27 MHz.
160	A_VDD	Power	3.3-V Analog PLL Power
161	DVD-DATA0 /CD-DATA	I	Serial CD data.This pin is shared with DVD compressed data DVD-DATA0.
162	DVD-DATA1 /CD-LRCK	I	Programmable polarity 16-bit word synchronization to the decoder (right channel HIGH).This pin is shared with DVD compressed data DVD-DATA1.
163	DVD-DATA2 /CD-BCK	I	CD bit clock.Decoder accept multiple BCK rates.This pin is shared with DVD compressed data DVD-DATA2.
164	DVD-DATA3 /CD-C2P0	I	Asserted HIGH indicates a corrupted byte.Decoder keeps the previous valid picture on-screen until the next valid picture is decoded.This pin is shared with DVD compressed data DVD-DATA3.
165	DVD-DATA4 /CDG-SDATA	I	DVD parallel compressed data from DVD DSP.Or CD+G(Subcode) data indicating serial subcode data input.
166	VSS	Ground	Ground for core logic and I/O signals
167	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
168	DVD-DATA5 /CDG-VFSY	I	DVD parallel compressed data from DVD DSP.Or CD+G(Subcode) Frame Sync indicating frame-start or composite synchronization input.
169	DVD-DATA6 /CDG-SOS1	I	DVD parallel compressed data from DVD DSP.Or CD+G(Subcode) Block Sync indicating block-start synchronization input.
170	DVD-DATA7 /CDG-SCLK	I	DVD parallel compressed data from DVD DSP.Or CD+G(Subcode) Clock indicating subcode data clock input or output.

2.Pin function   4/4

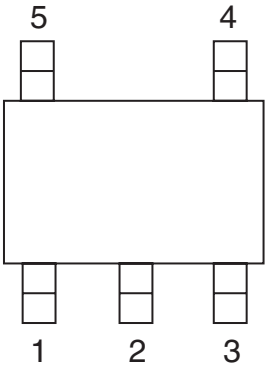| Pin No.	Symbol	I/O	Function
171	VDACK	I	In synchronous mode,bitstream data acknowledge.Asserted when DVD data is valid.Polarity is programmable.
172	VREQUEST	O	Bitstream request.Decoder asserts VREQUEST to indicate that the bitstream input buffer has available space.Polarity is programmable.
173	VSTROBE	I	Bitstream strobe.Programmable dual mode pulse.Asynchronous and synchronous.In Asynchronous mode,an external source pulses VSTROBE to indicate data is ready for transfer.In synchronous mode,VSTROBE clocks data.
174	ERROR	I	Error in input data.If ERROR signal is not available from the DSP it must be grounded.
175	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
176	RESERVED	I	Tie to VSS or VDD_3.3 as specified in Table 1.
177	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
178	VSS	Ground	Ground for core logic and I/O signals
179	NC	O	No connect.
180	RESERVED	I	Tie to VSS or VDD_3.3 as specified in Table 1.
181	NC	O	No connect.
182~184	HADDR0~2	I	Host address bus.3-bit address bus selects one of eight host interface registers.
185~187	RESERVED	I	Tie to VSS or VDD_3.3 as specified in Table 1.
188	VSS	Ground	Ground for core logic and I/O signals
189	VDD_2.5	Power	2.5-V supply voltage for core logic
190	RESERVED	I	Tie to VSS or VDD_3.3 as specified in Table 1.
191	VSS	Ground	Ground for core logic and I/O signals
192	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
193~196	RESERVED	I	Tie to VSS or VDD_3.3 as specified in Table 1.
197	HDATA7	I/O	HDATA(7~0) is the 8-bit bi-directional host data bus through which the host writes data to the decoder Code FIFO.MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM/ROM via HDATA(7~0).
198	VSS	Ground	Ground for core logic and I/O signals
199~203	HDATA6~2	I/O	HDATA(7~0) is the 8-bit bi-directional host data bus through which the host writes data to the decoder Code FIFO.MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM/ROM via HDATA(7~0).
204	VDD_3.3	Power	3.3-V supply voltage for I/O signals.
205	VSS	Ground	Ground for core logic and I/O signals
206~207	HDATA1,0	I/O	HDATA(7~0) is the 8-bit bi-directional host data bus through which the host writes data to the decoder Code FIFO.MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM/ROM via HDATA(7~0).
208	CS	I	Host chip select Host asserts CS to select the decoder for a read or write operation.The falling edge of this signal triggers the read or write operation.

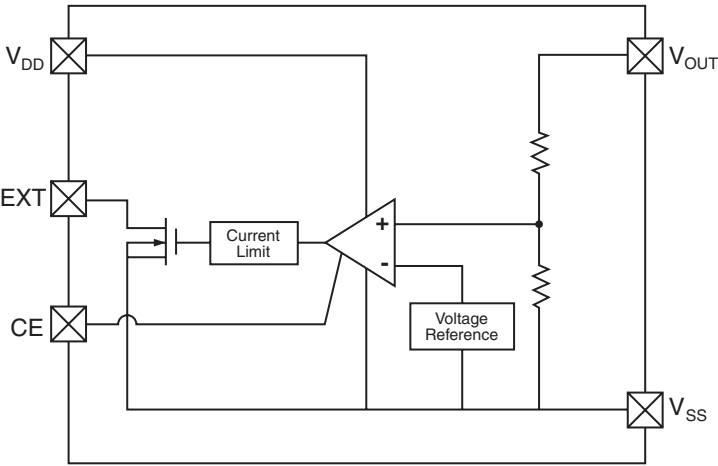## ■ TK11140SC-W (IC485) : Regulator

1.Pin layout

on / off control	1	6	Vin
GND	2		
Np (Vref)	3	4	Vout

2.Block diagram

VIN

Thermal Sensor

Rin=550kΩ

on / off Ccont.

Bandgap Reference

Cnp

VOUT

GND

■ XC62ER3602M-X (IC400) : Regulator

1.Pin layout

5   4

1   2   3

2.Block diagram

V_{DD}

EXT

CE

Current Limit

+
−

Voltage Reference

V_{OUT}

V_{SS}

3.Pin function

Pin No.	Symbol	Function
1	V_{SS}	GND
2	V_{IN}	Power supply input
3	V_{OUT}	Regulator output
4	EXT	Base current control terminal
5	CE	Chip enable

< **M E M O** >

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